

Domino\_BA  
Schematics Document

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<Variant Name>

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Title

Cover Page

Size

Document Number

Rev

A3

Domino

-1

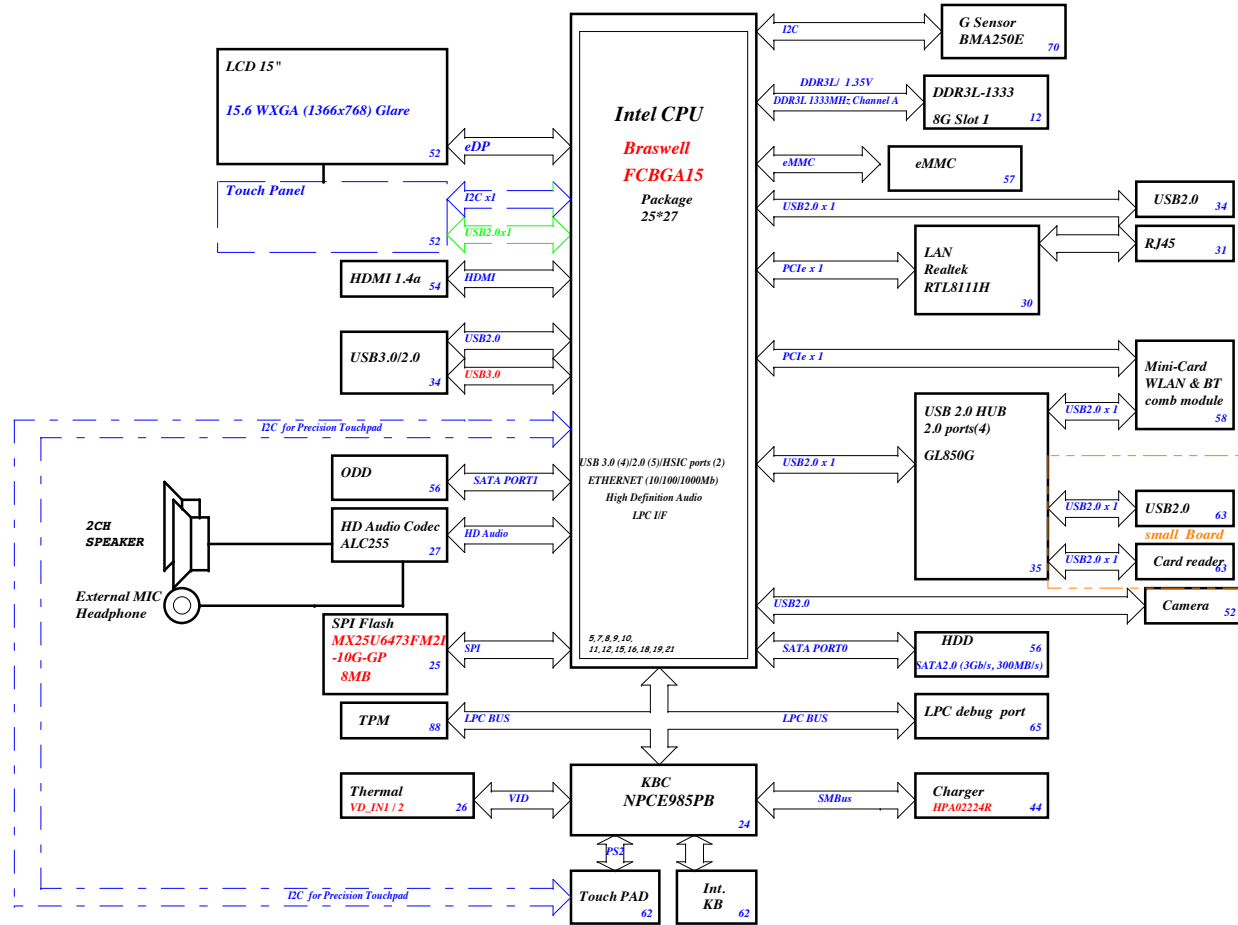
Date: Friday, March 20, 2015

Sheet 1 of 102

# Domino\_BA Board Block Diagram

Project code : 4PD053010001  
PCB P/N : 14285  
Revision : -1

CHARGER	
HPA02224	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
RT6575D	45
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5
CPU DC/DC	
NCP81201MNTXG	46-47
INPUTS	OUTPUTS
DCBATOUT	1V_CPU_CORE
CPU DC/DC	
NCP81201MNTXG	48
INPUTS	OUTPUTS
DCBATOUT	6FX_CORE
SYSTEM DC/DC	
TPS51716	50
INPUTS	OUTPUTS
DCBATOUT	1D05V_S5
SYSTEM DC/DC	
TPS51716	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_CPU_VDDQ_S5
SYSTEM LDO	
S-1339D15	51
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
SYSTEM LDO	
RT9043GB	51
INPUTS	OUTPUTS
1D8V_S5	1D24V_S5
SYSTEM DC/DC	
RT8068AZQWID	51
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5



PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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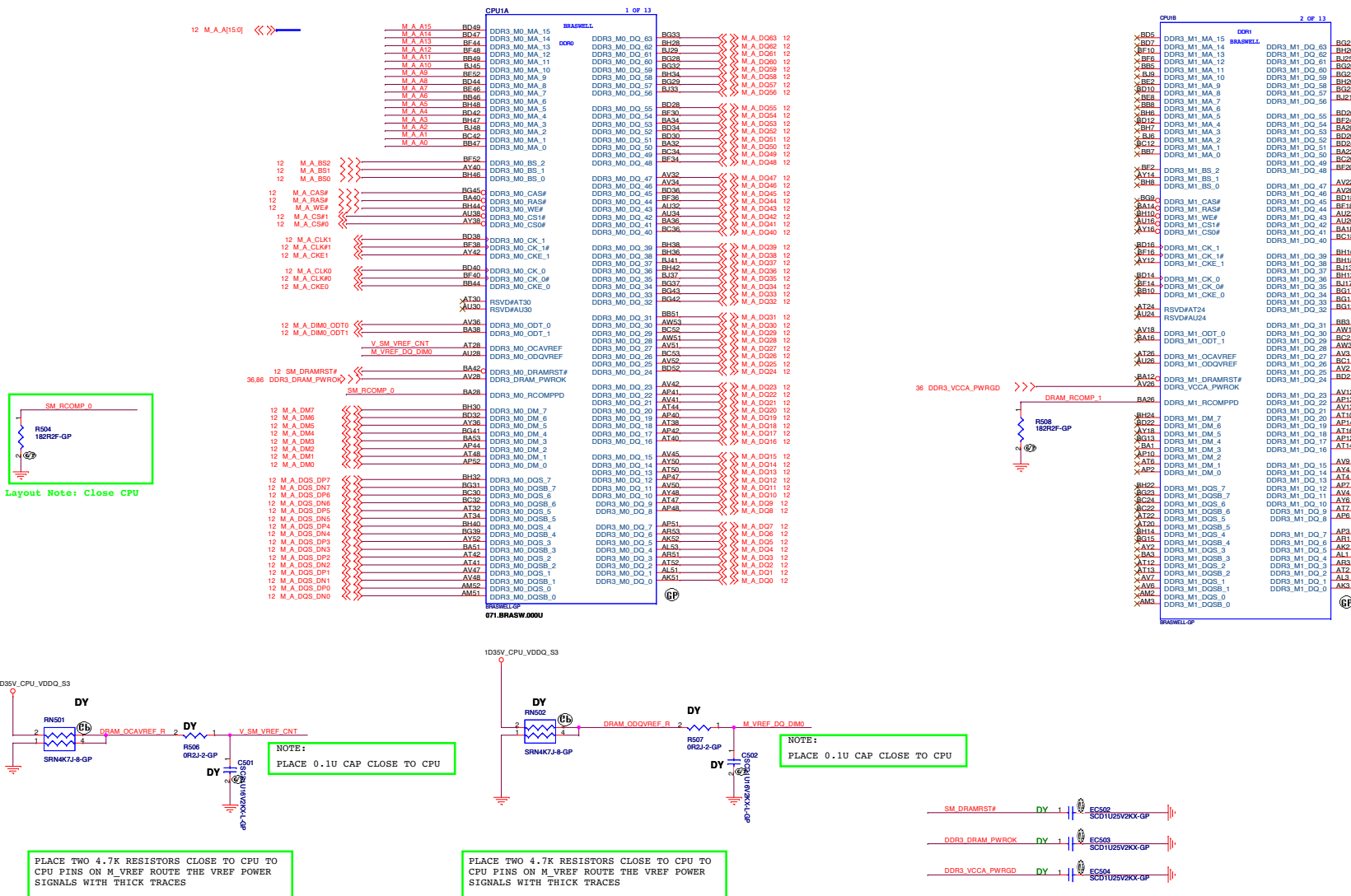
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Sheet 4 of 102



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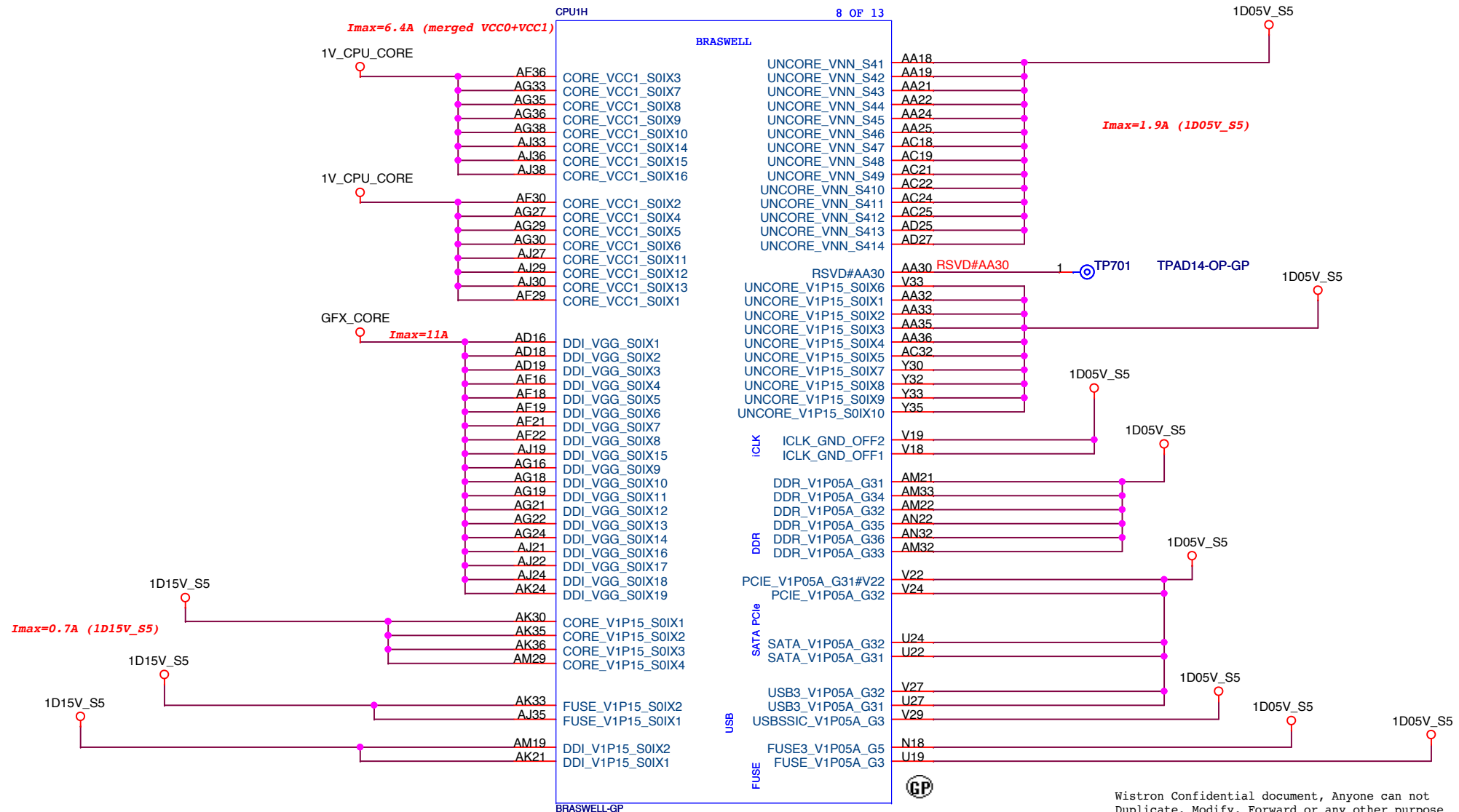
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A4	Domino	-1
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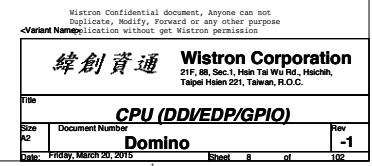
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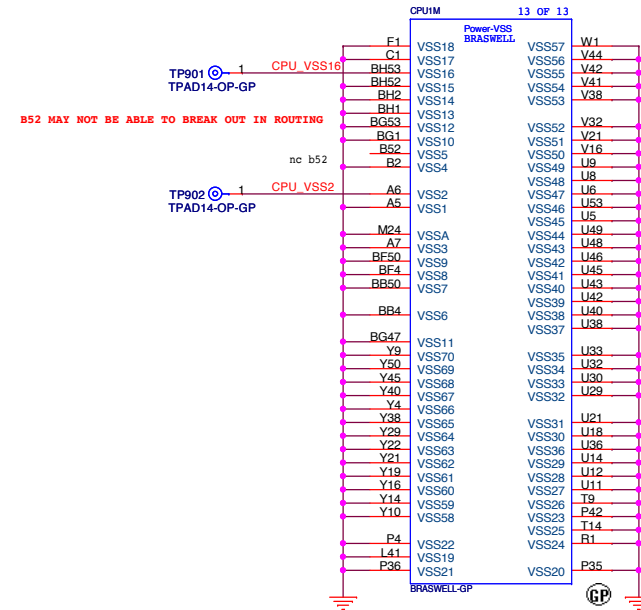
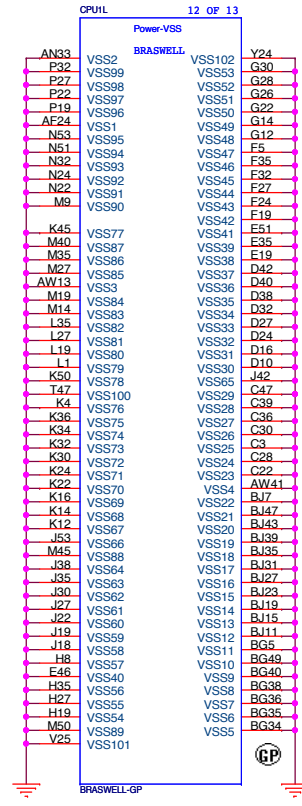
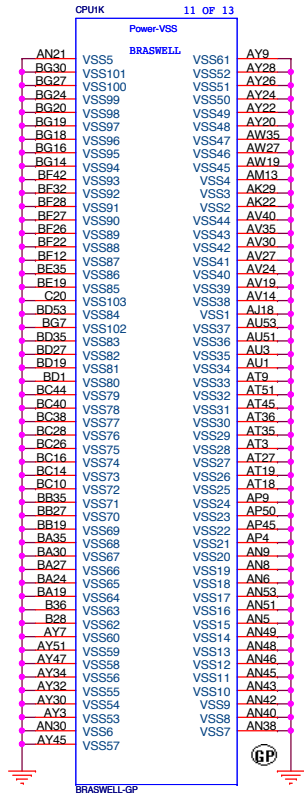
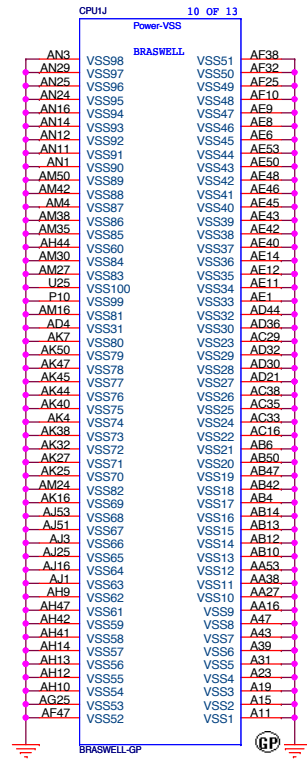
Sheet 7 of 102





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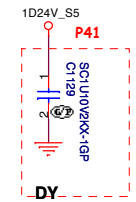
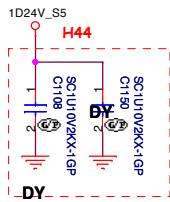
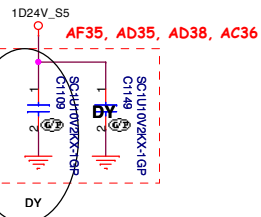
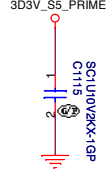
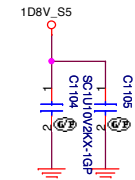
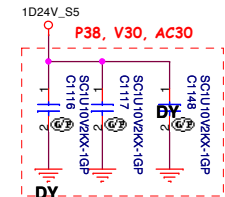
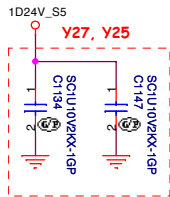
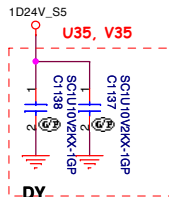
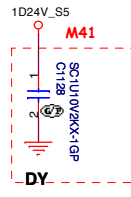
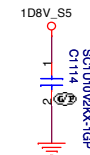
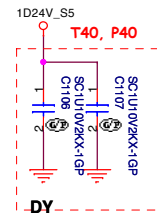
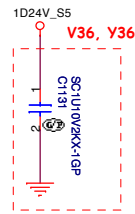
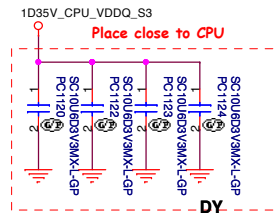
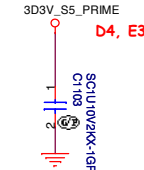
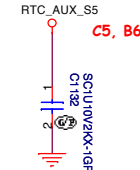
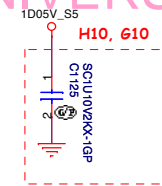
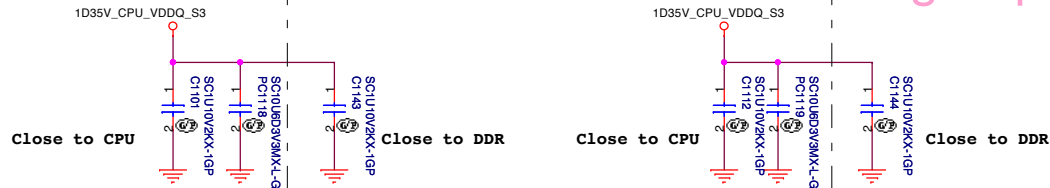
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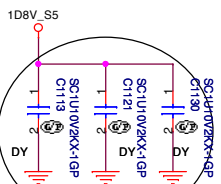


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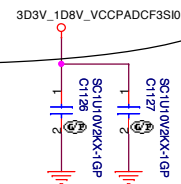
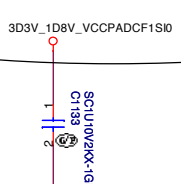
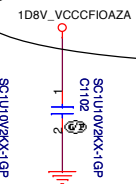
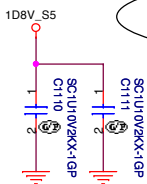
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20150302 SC



20150313 SC



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Title			
CPU (Power CAP2)			
Size A3	Document Number		Rev
Domino		-1	
Date:	Friday, March 20, 2015	Sheet 11 of	102

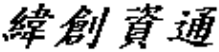


SSID = MEMORY

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Date: Friday, March 20, 2015		Sheet 14 of 102

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC  
SHOULD BE PLACED OUTSIDE KOZ AREA

All the straps are sampled on the rising edge of the  
PMC\_RSMRST\_N signal (check list)

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Description	DDI0_Detected	DDI1_Detected	A16 Swap Override	DSI Display Detected	Boot BIOS Strap BBS	Flash Descriptor Security Override	DFX Boot Halt Strap & VISA Early POSM Debug Enable	DFX Sus Debug Strap	ICLK, USB2, DDI SFR Supply Select	ICLK SFR Bypass	POSM Select	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC bypass
GPIO	GPIO_SUS0	GPIO_SUS1	GPIO_SUS2	GPIO_SUS3	GPIO_SUS4	GPIO_SUS5	GPIO_SUS6	GPIO_SUS7	SEC_GPIO_SUS8	SEC_GPIO_SUS9	SEC_GPIO_SUS10	GP_CAMERA8B08	GP_CAMERA8B09	GP_CAMERA8B11
Schematic														
High	DDI0 Detect	DDI1 Detect	Normal Operation	DSI Detect	Boot from SPI	Weak internal pull-up Normal operation	Normal	Weak internal pull-up Normal	1.35V	Weak internal pull-up Bypass with 1.05V	PMC	Bypass	Bypass	Bypass
Low	Disable	Disable	Change Boot Loader address (A16 Override)	Disable	Boot from LPC	Override	Halt boot enable	Sus Debug enable	1.25V	No bypass	Fuse controller	No bypass	No bypass	No bypass

Table 29. Straps (Sheet 1 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[0]	DDI0 Detect	Weak internal pull-down	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
GPIO_SUS[1]	DDI1 Detect	Weak internal pull-down	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
GPIO_SUS[2]	A16 swap override	Weak internal pull-up	Top Swap (A16 Override) 0 = Change Boot Loader address. 1 = Normal Operation
GPIO_SUS[4]	Boot BIOS Strap BBS	Weak internal pull-up	BIOS Boot Selection 0 = - 1 = SPI
GPIO_SUS[5]	Flash Descriptor Security Override	Weak internal pull-up	Security Flash Descriptors 0 = Override 1 = Normal Operation

Table 29. Straps (Sheet 2 of 2)

Signal Name	Purpose	Pull-Up/Pull-Down	Strap Description
GPIO_SUS[6]	ICLK, USB2, DDI SFR Supply Select	Weak internal pull-down	0 = Supply is 1.25V 1 = Supply is 1.25V This strap also contains PLL LDO 0: supply is 1.25V; 1: supply is 1.35V. Selects supply voltage for LDOs used for PLLs, thermal oscillators, USB2, ICLK and DDI
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	Weak internal pull-up	0 = No bypass 1 = Bypass with 1.05V
GPIO_SUS[10]	POSM Select	Weak internal pull-down	Selects which POSM will be observed at time 0 0 = Fuse controller 1 = PMC
GPIO_CAMERA8B08	ICLK Xtal OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERA8B08	CCU SUS RO Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass
GPIO_CAMERA8B11	RTC OSC Bypass	Weak internal pull-down	0 = No Bypass 1 = Bypass

CHV Straps [CRB] -- strap detect @ RSMRST# assertion				
Purpose	CHV Pin Name [refer CHV symbol PIN]	PU/PD (internal - Weak)	Options	Default State on board?
DDI0 Detected	GPIO_SUS0	PD	1- DDI0 Detect, 0- Disable	High
DDI1 Detected	GPIO_SUS1	PD	1- DDI1 Detect, 0- Disable	High
A16 swap override	GPIO_SUS2	PU	1- Default, 0- A16 override	High
DSI Display Detected	GPIO_SUS3	PD	1- DSI detect, 0- Disable	Low
Boot BIOS Strap BBS	GPIO_SUS4	PU	1- Boot from SPI, 0- Boot from LPC	High
Flash Descriptor Security Override	GPIO_SUS5	PU	1- Security enabled, 0- Security disabled	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	PU	1- normal, 0- Halt boot enable	High
DFX Sus Debug Strap	GPIO_SUS7	PU	1- Normal, 0- Sus Debug enable	High
ICLK, USB2, DDI SFR Supply Select	SEC_GPIO_SUS8	PU	1- 1.35V, 0- 1.25V	Low
ICLK SFR Bypass	SEC_GPIO_SUS9	PD	1- Bypass with 1.05V, 0- No Bypass	Low
POSM Select	SEC_GPIO_SUS10	PD	1- PMC, 0- Fuse controller	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERA8B08	PD	1- Bypass, 0- No bypass	Low
CCU SUS RO Bypass	GP_CAMERA8B09	PD	1- Bypass, 0- No bypass	Low
RTC OSC Bypass	GP_CAMERA8B11	PD	1- Bypass, 0- No bypass	Low



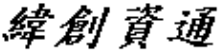


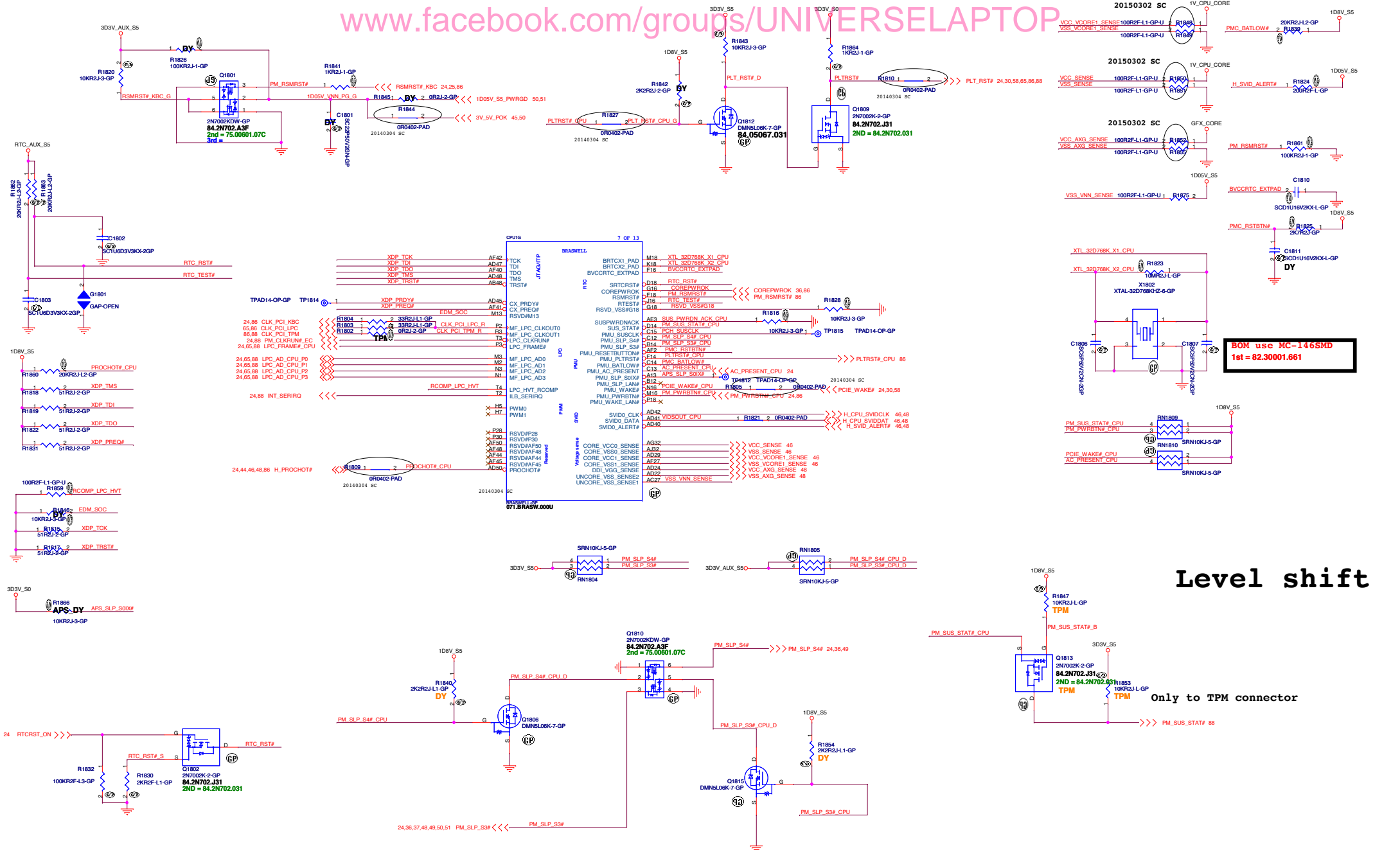
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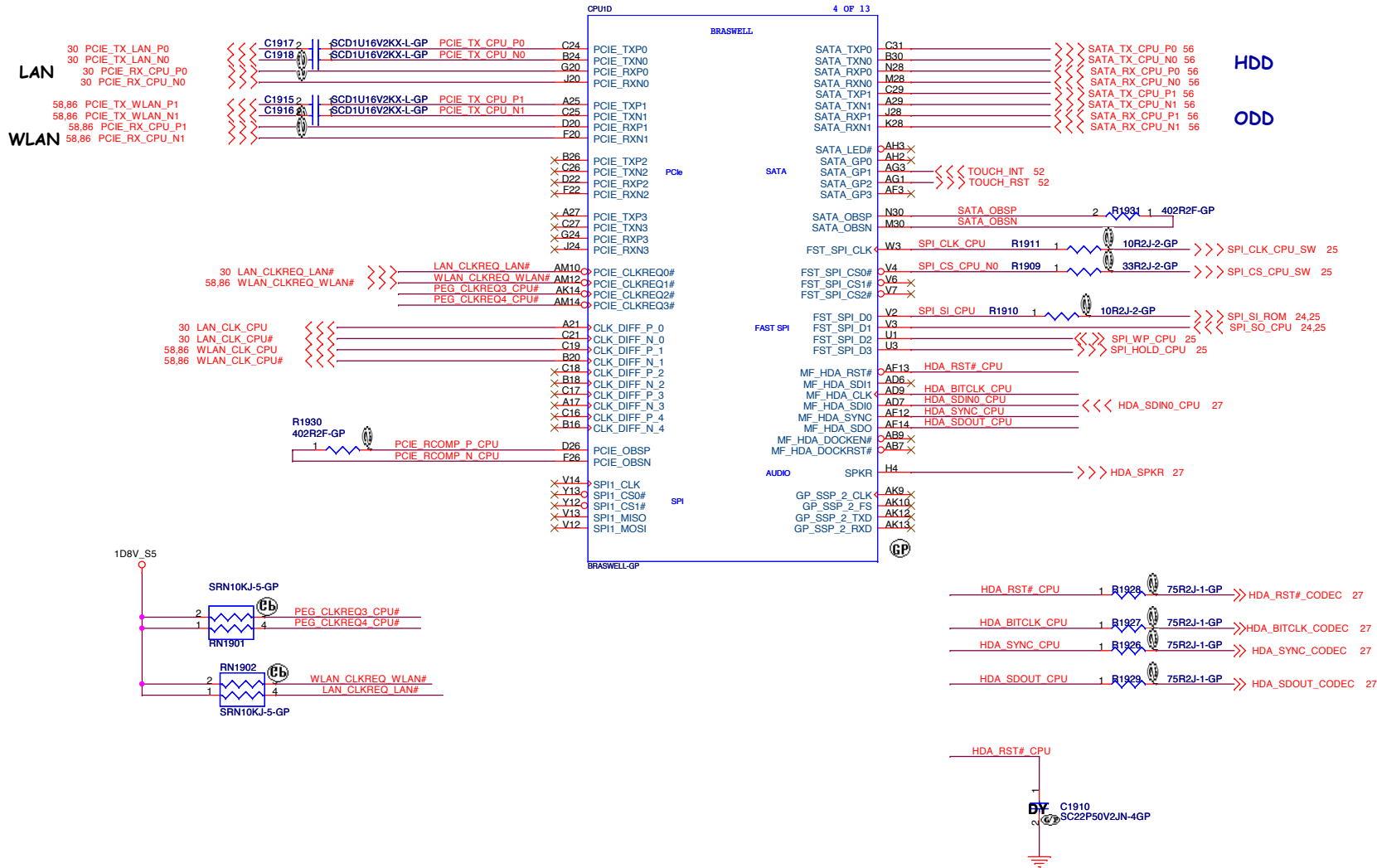
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Level shift

Only to TPM connector



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Title CPU (SATA/PCIE/HDA)			
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SSID = PCH

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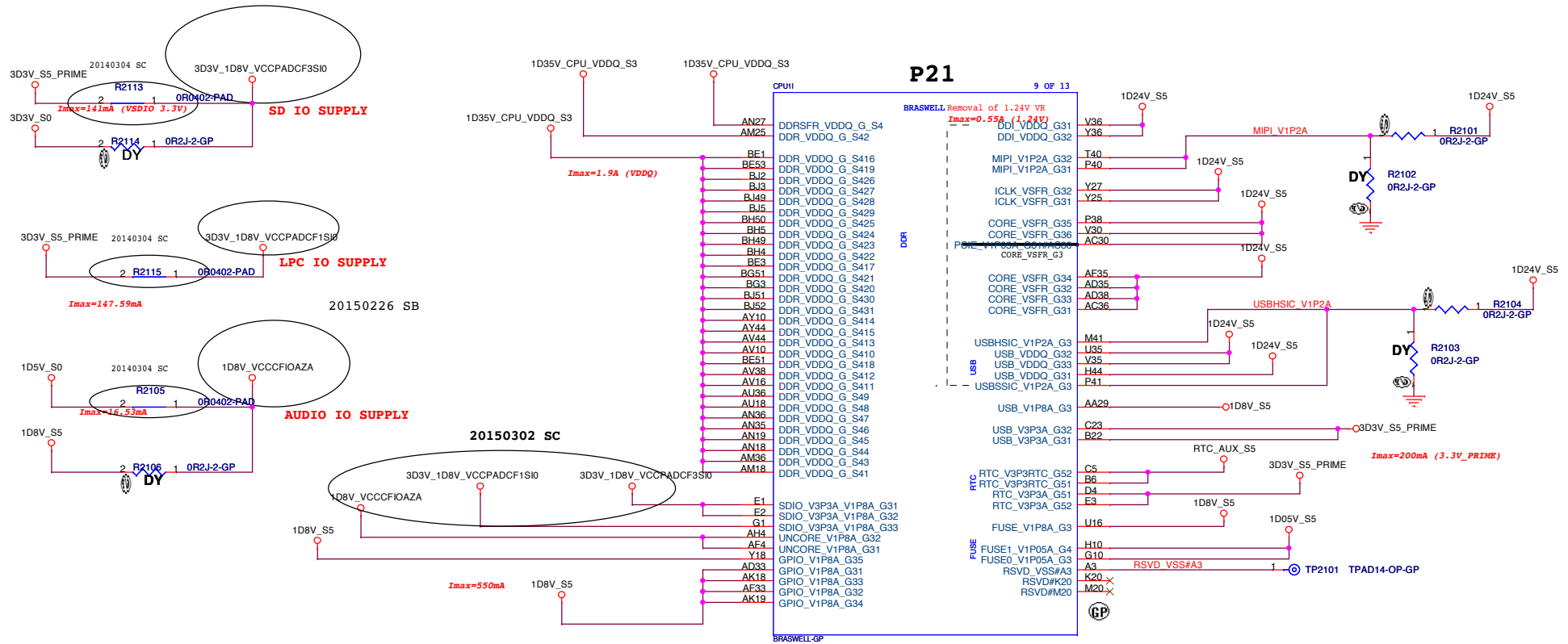
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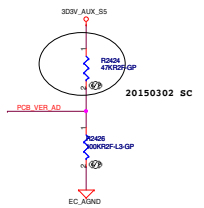
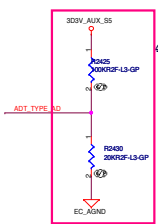
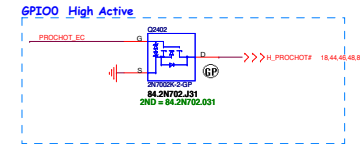
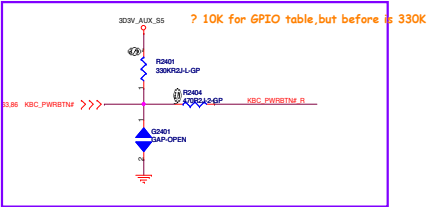
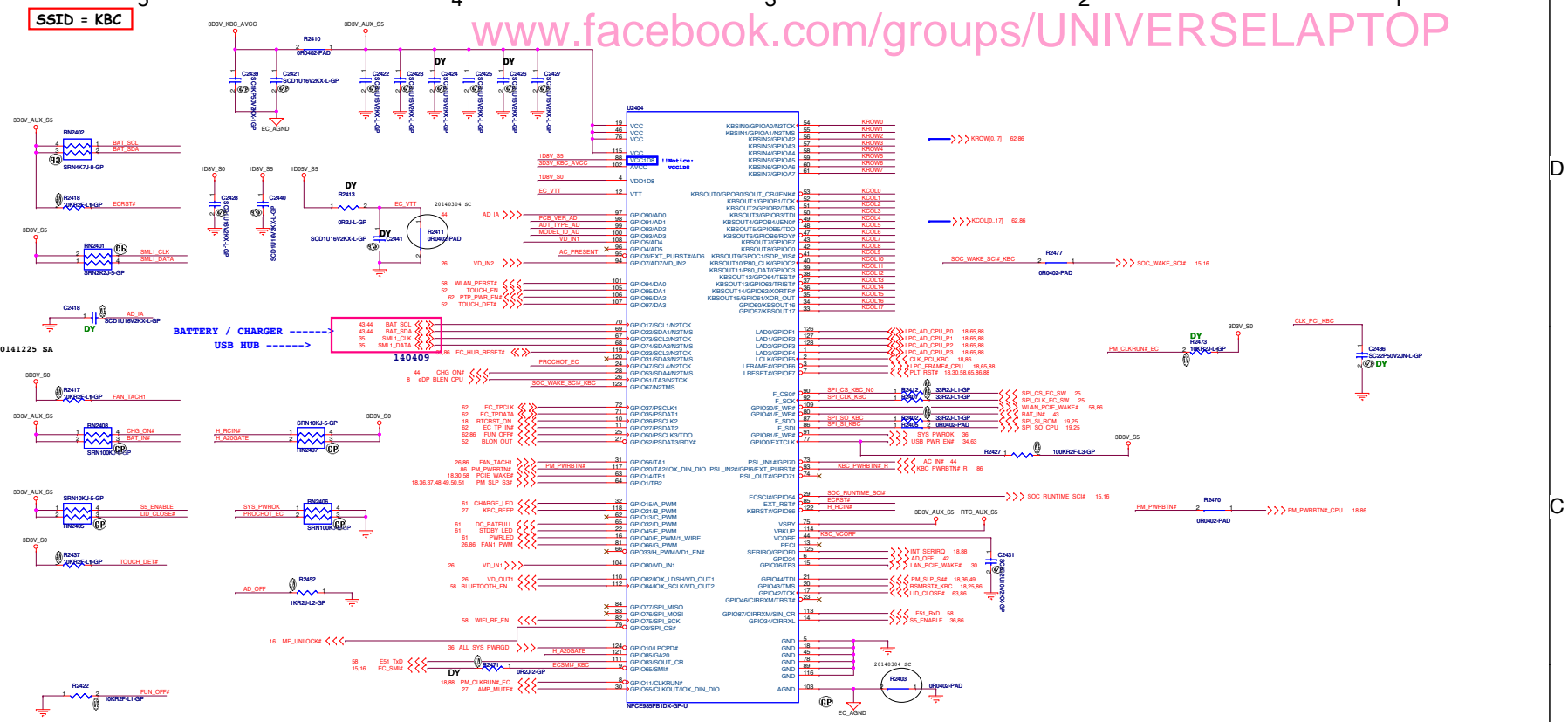
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Date: Friday, March 20, 2015	Sheet 23 of	102

SSID = KBC

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PCH_VDD_50			
Pin	Pin Load Register	Pin High Register	PCH Pinmux Setting
5A	100.0 K	10.0 K	
5B	100.0 K	20.0 K	+2.875 V
5C	100.0 K	32.0 K	+2.875 V
Reserved for product use	100.0 K	47.0 K	+2.875 V
Reserved for product use	100.0 K	64.9 K	+2.875 V
Reserved for product use	100.0 K	76.8 K	+2.875 V
PCH_VDD_10			
Pin	Pin Load Register	Pin High Register	PCH Pinmux Setting
10A	100.0 K	10.0 K	
10B	100.0 K	20.0 K	+2.875 V
10C	100.0 K	32.0 K	+2.875 V
Reserved for product use	100.0 K	47.0 K	+2.875 V
Reserved for product use	100.0 K	64.9 K	+2.875 V
Reserved for product use	100.0 K	76.8 K	+2.875 V
PCH_VDD_15			
Pin	Pin Load Register	Pin High Register	PCH Pinmux Setting
15A	100.0 K	10.0 K	
15B	100.0 K	20.0 K	+2.875 V
15C	100.0 K	32.0 K	+2.875 V
Reserved for product use	100.0 K	47.0 K	+2.875 V
Reserved for product use	100.0 K	64.9 K	+2.875 V
Reserved for product use	100.0 K	76.8 K	+2.875 V

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Variant Name: KBC NPCE985

Model Name: Domino

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Page: 25 of 108



**SPI FLASH ROM (8M byte) for PCH**

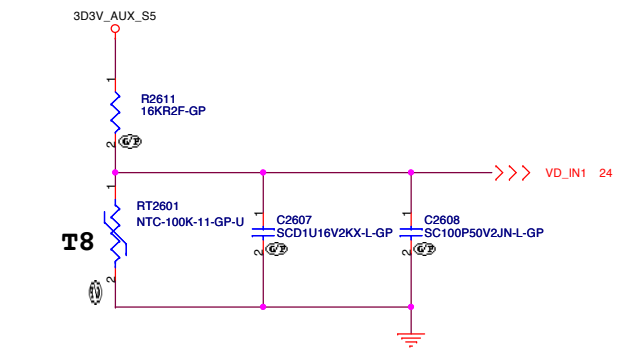
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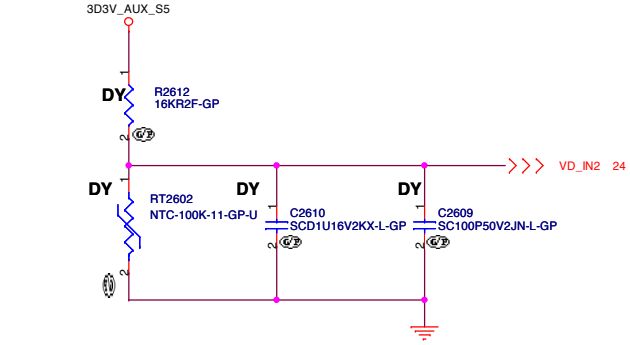
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Size A3	Document Number		Rev
	<b>Domino</b>		<b>-1</b>
Date:	Friday, March 20, 2015	Sheet 25 of	102

SSID = Thermal

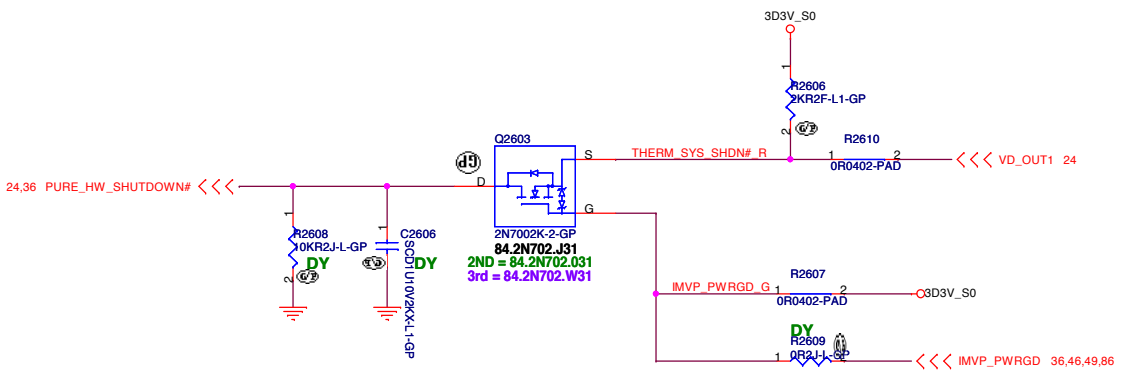
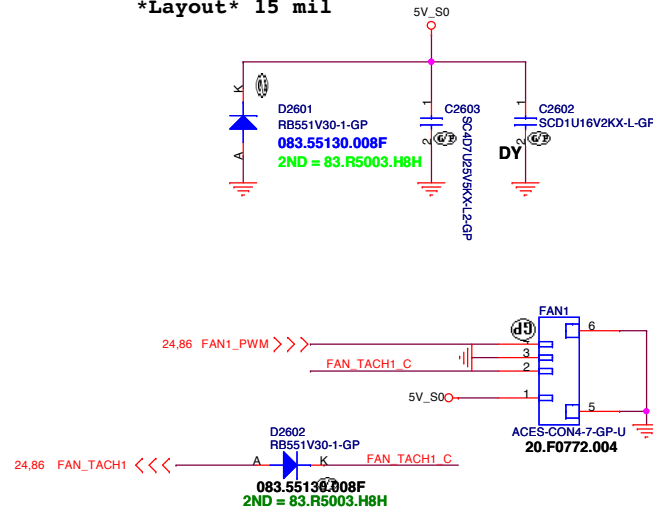
\*Layout\* 15 mil



PT2601 close CPU and Vcore chock



PT2602 close CPU and memory



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Date: Friday, March 20, 2015		Rev -1	
Sheet 26 of 102		Thermal 7718/Fan Contrllor P2793	
Domino			



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***Reserved***

Size  
A4

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**Domino**

Rev  
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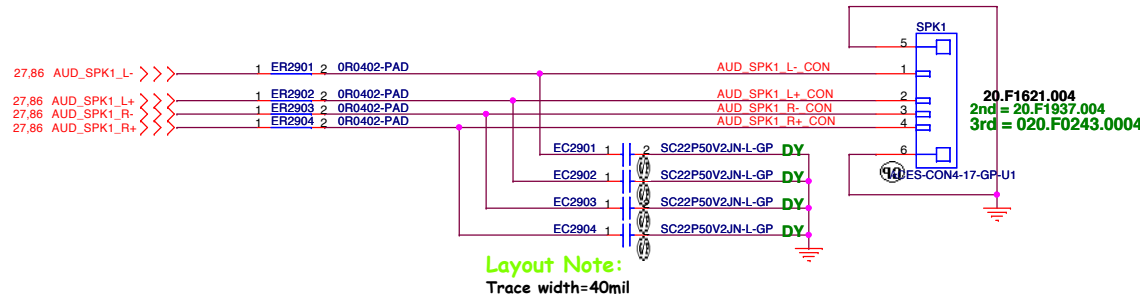
Date: Friday, March 20, 2015

Sheet 28 of 102

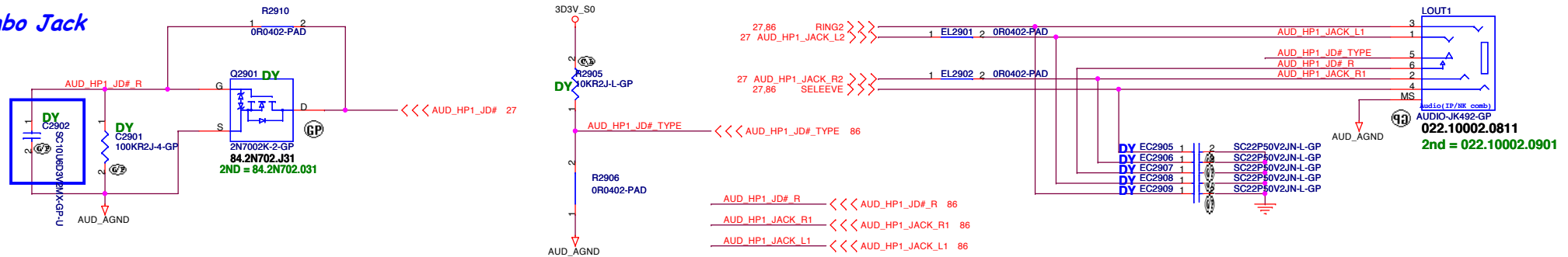
SSID = AUDIO

Speaker

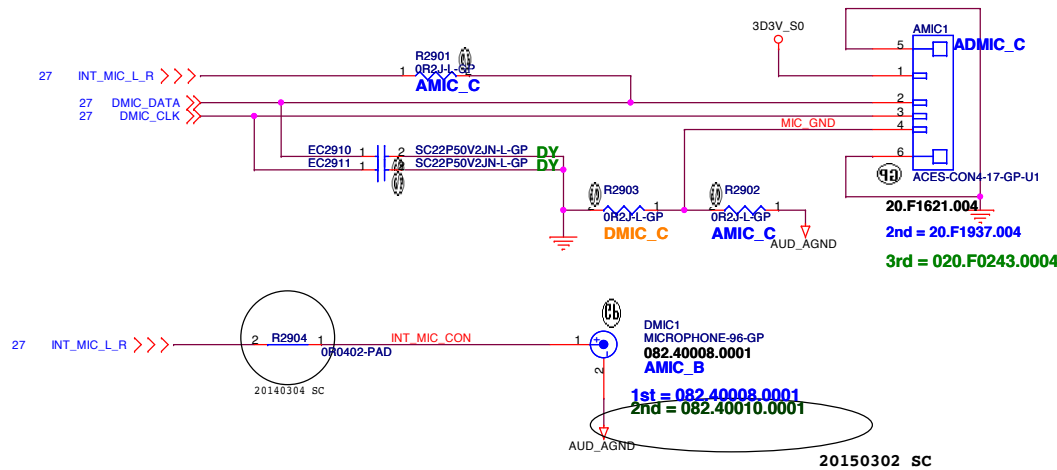
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### Combo Jack



### DMIC AMIC



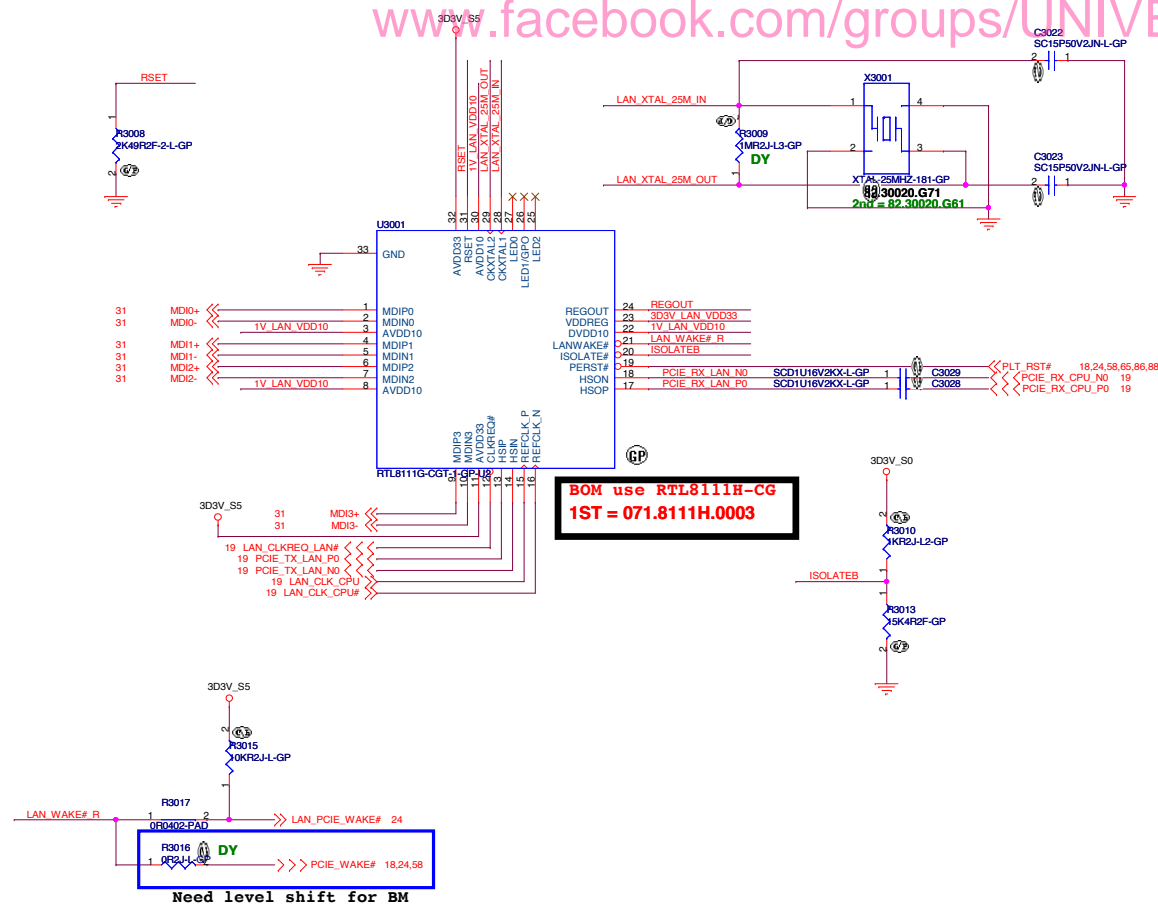
AMIC on board: mount DMIC1, R2904, DY AMIC1, R2901, R2902, R2903, EC2910, EC2911  
 AMIC for cable: mount AMIC1, R2901, R2902, DY R2903, EC2910, EC2911, DMIC1, R2904  
 DMIC for cable: mount AMIC1, R2903, DY R2901, R2902, EC2910, EC2911, DMIC1, R2904

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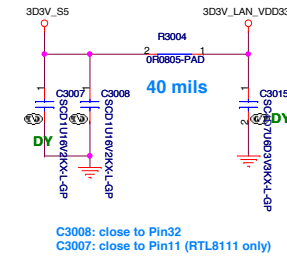
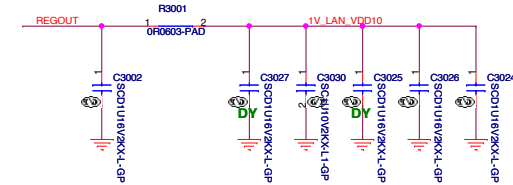
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Title	Audio Jack		
Size	Document Number	Rev	
Custom	Domino	-1	
Date:	Friday, March 20, 2015	Sheet 29	of 102



Layout:  
For RTL8111G(S)  
\* Place C3021 to C3024 close to each VDD10 pin--3, 8,

C3024: close to Pin8  
C3025: close to Pin30  
C3026: close to Pin3  
C3027: close to Pin22

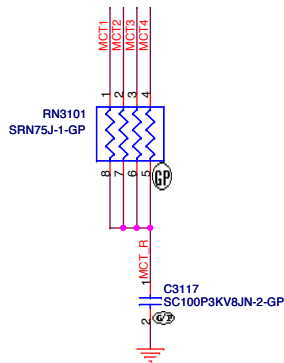
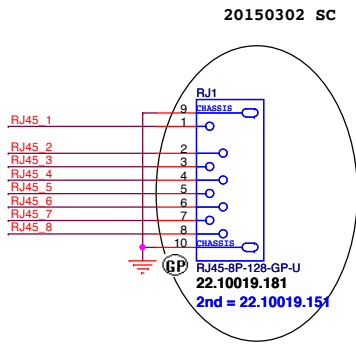
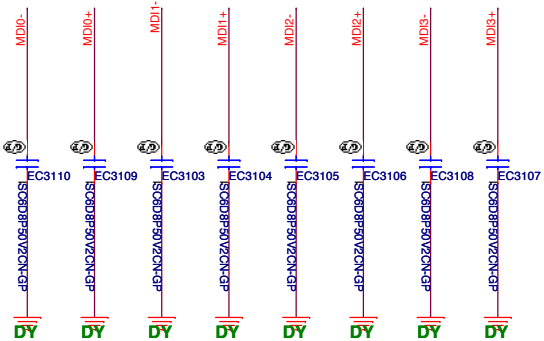
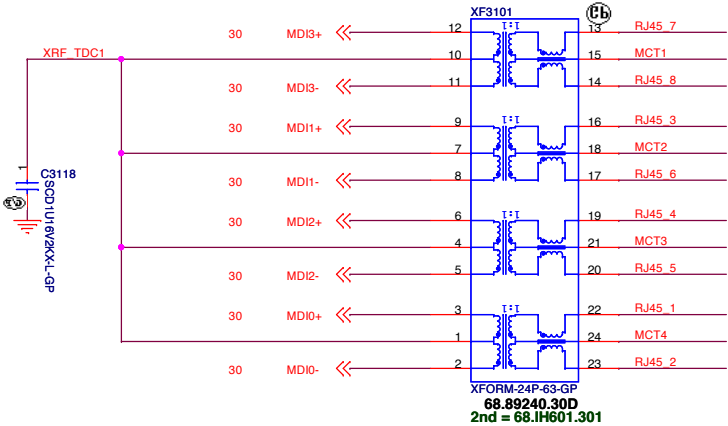


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Title <b>LAN(RTL8111)</b>			
Size	Document Number	Rev	
Custom		<b>Domino</b>	<b>-1</b>
Date:	Friday, March 20, 2015	Sheet	30 of 102

SSID = LAN



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Title

RTS5170(CARD READER)

Size A4

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Sheet 32 of 102



SSID = SDIO

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# SD//MS Card Reader

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Title

**CARD Reader CONN**

Size Custom

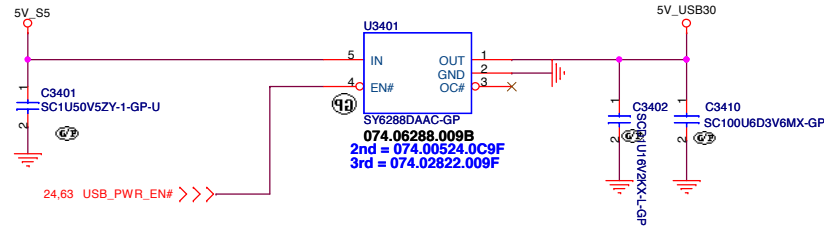
Document Number  
**Domino**

Rev  
**-1**

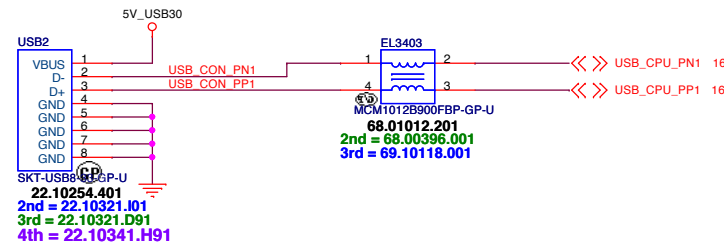
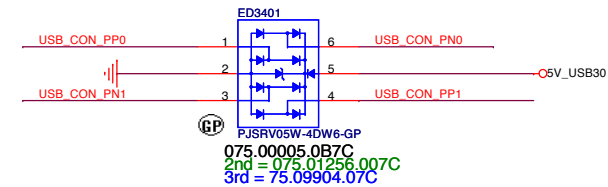
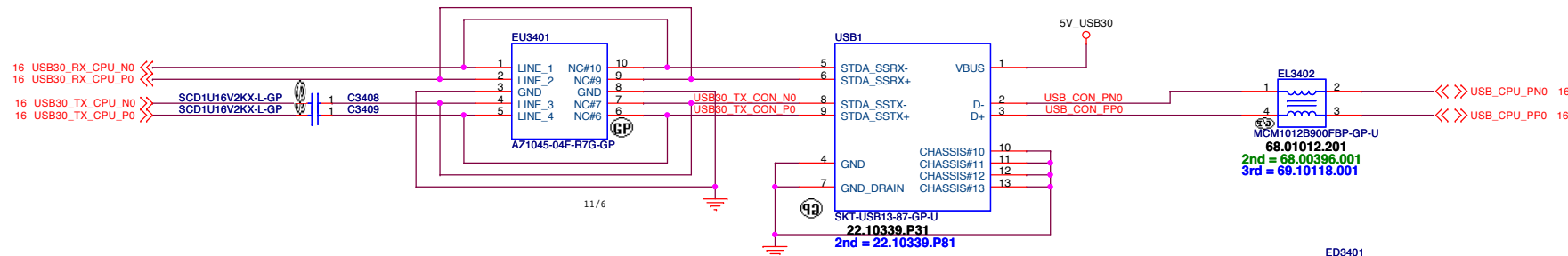
Date: Friday, March 20, 2015

Sheet 33 of 102

### Low Active 2A

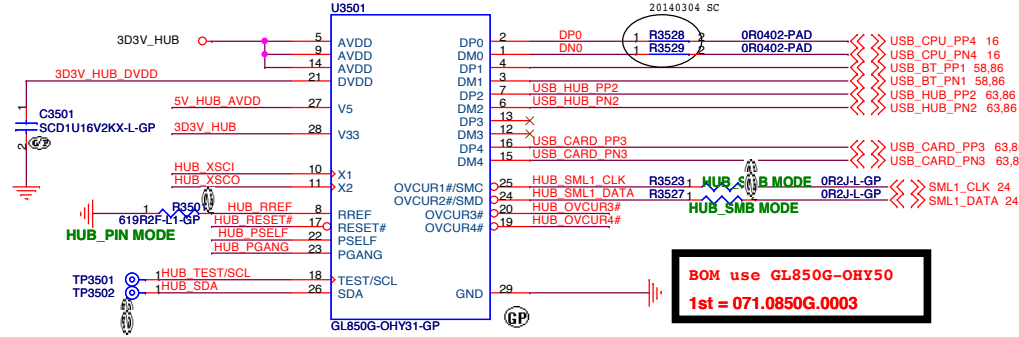
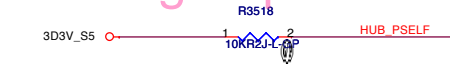
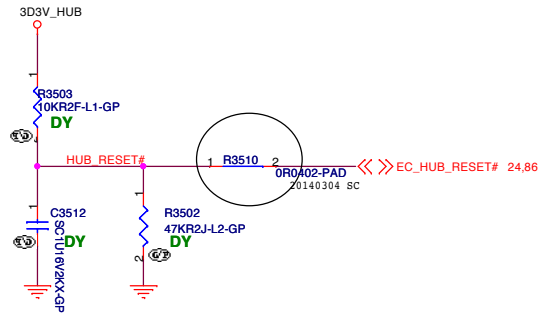


USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+



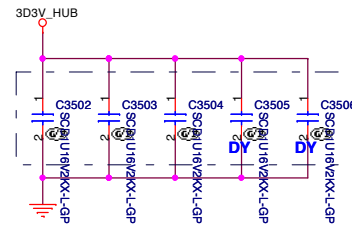
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Title: <b>USB 2.0 / 3.0 Port</b>	
Size: A3	Document Number: <b>Domino</b>
Date: Friday, March 20, 2015	Sheet 34 of 102
Rev: <b>-1</b>	

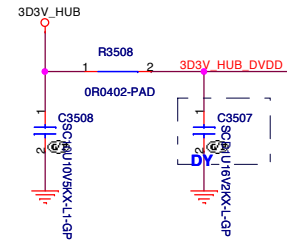


BOM use GL850G-OHY50  
1st = 071.0850G.0003

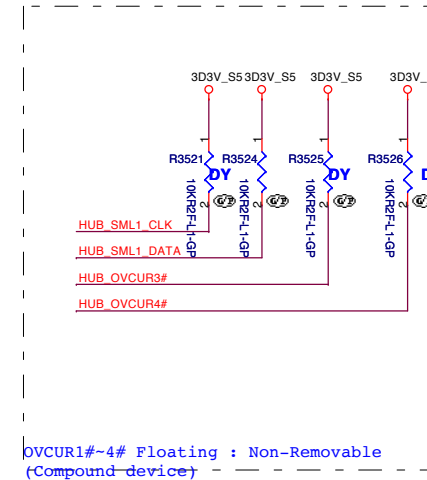
CPU  
WLAN(Bluetooth)  
USB 2.0(SMBD)  
not use  
Card reader



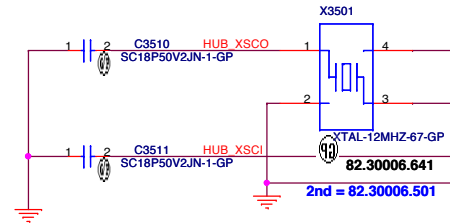
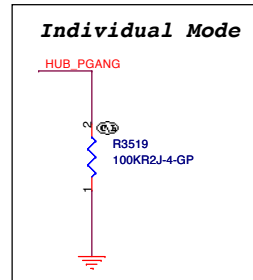
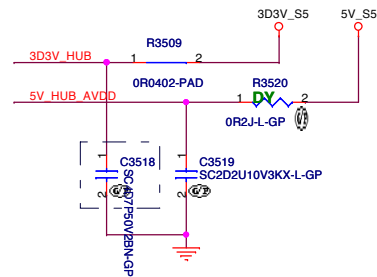
As close to GL850G-32



EC1 close to  
PIN28



OVCUR1#~4# Floating : Non-Removable  
(Compound device)



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Title

USB HUB

Size

Document Number

Custom

Domino

Date: Friday, March 20, 2015

Sheet 35

of

Rev

-1

Power Sequence

Table 55. S4/S5 to S0 (Power Up) Sequence

Parameter		Min	Max	Unit	Notes
T0	RTC_VCC to ILB_RTC_TEST# de-assertion	9		ms	
T1	V3P3A valid to PMC_RSMRST# de-assertion	10		us	
T2	Core well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion	100		ms	
T3					

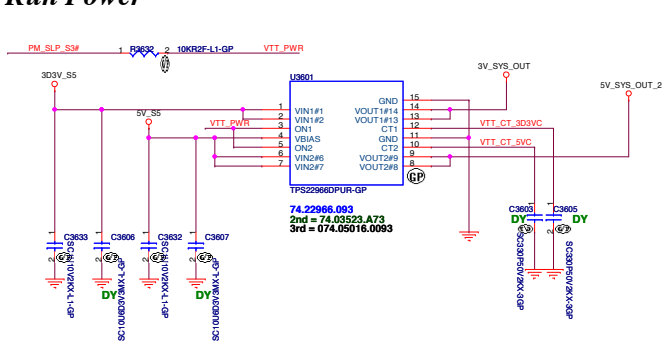
From EC

Delay 104ms with ALL\_SYS\_PWRGO

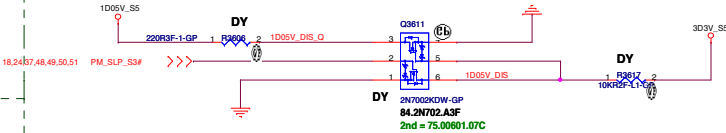
COREPWROK

DDR3\_DRAM\_PWROK

ANNIE Run Power

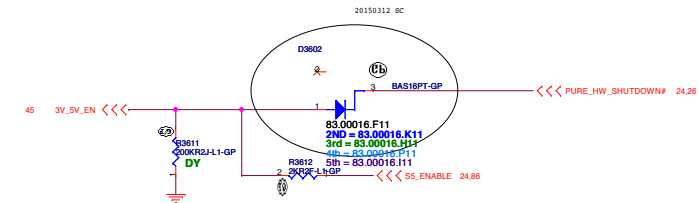
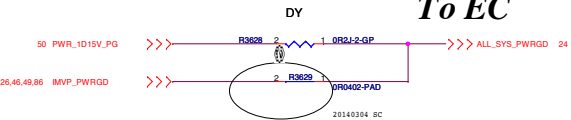


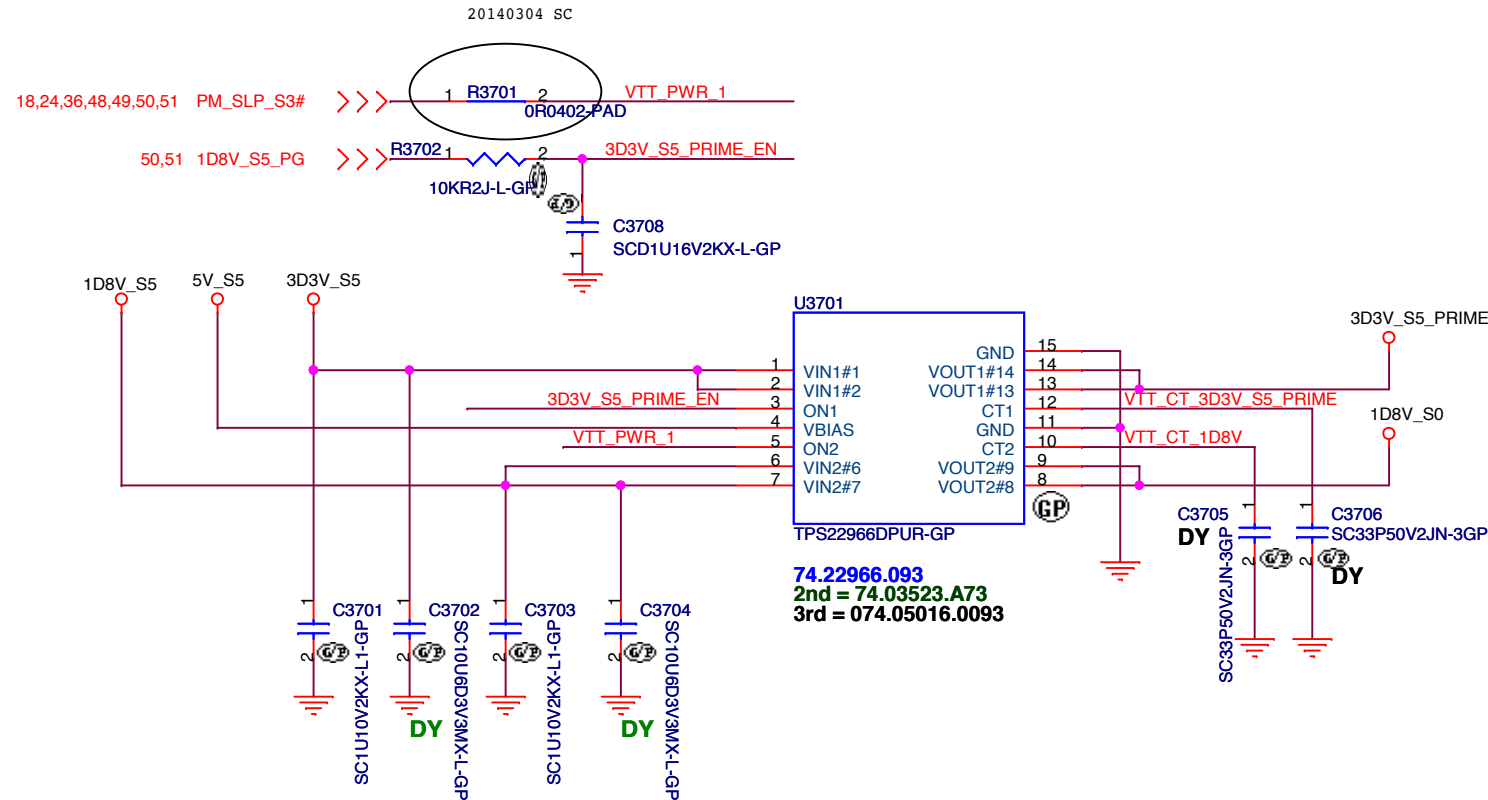
Discharge circuit



ALL\_SYS\_PWRGD

To EC





<Variant Name>

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Title

**ADAPTER OCP / S3 reduction**

Size  
A4

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Sheet 37 of 102

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**Reserved**

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A4

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**Domino**

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Sheet 38 of 102

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Size A4	Document Number <b>Domino</b>		Rev <b>-1</b>
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TitleReserved		
SizeA3	Document NumberDomino	Rev-1
Date: Friday, March 20, 2015	Sheet1	40 of 102

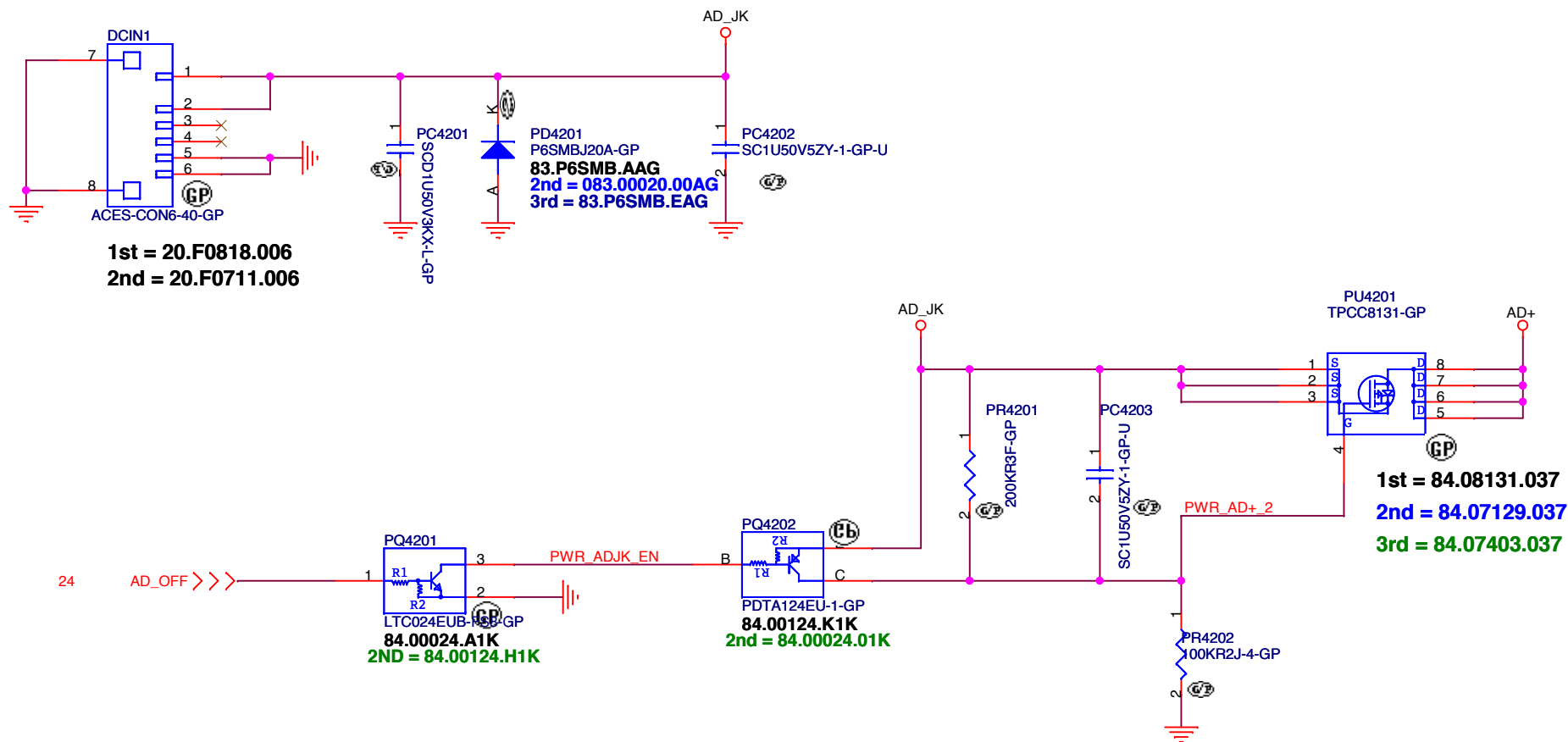


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Date: Friday, March 20, 2015		Sheet 41 of 102

## Adaptor in to generate DCBATOUT



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Title

DCIN JACK

Size

Document Number

Rev

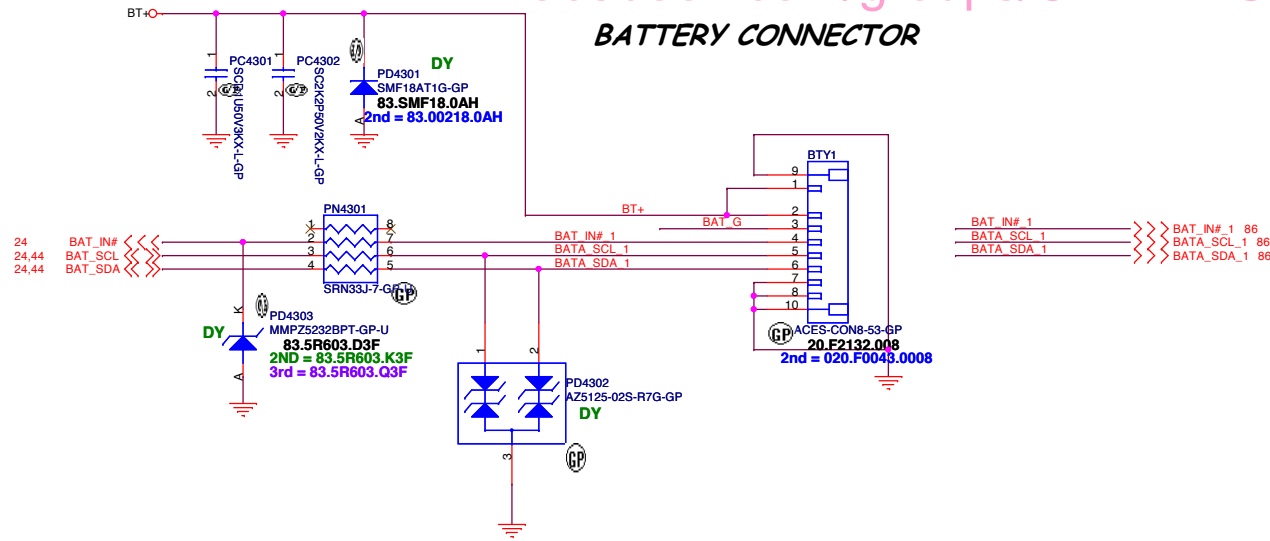
Domino

-1

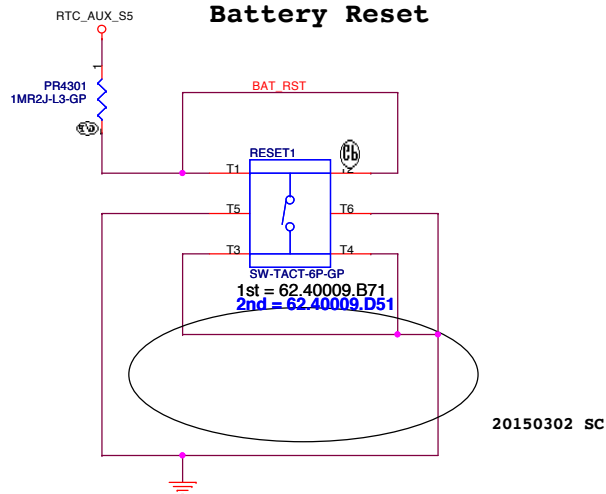
Date: Friday, March 20, 2015

Sheet 42 of 102

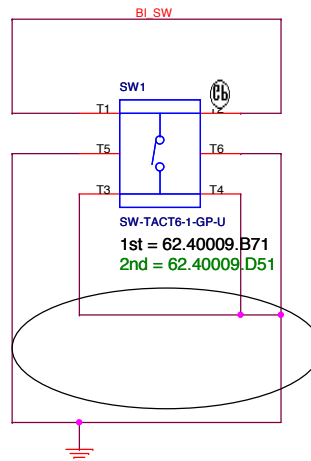
# BATTERY CONNECTOR



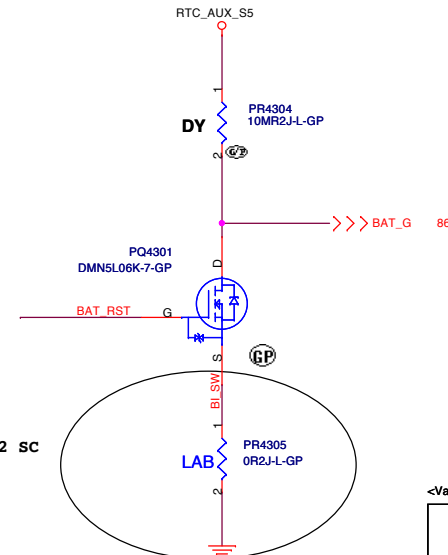
## Battery Reset



## Battery Insert



20150302 SC



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Title			BATT CONN	
Size	Document Number	Rev		-1
A3	Domino			
Date:	Friday, March 20, 2015	Sheet	43	of 102

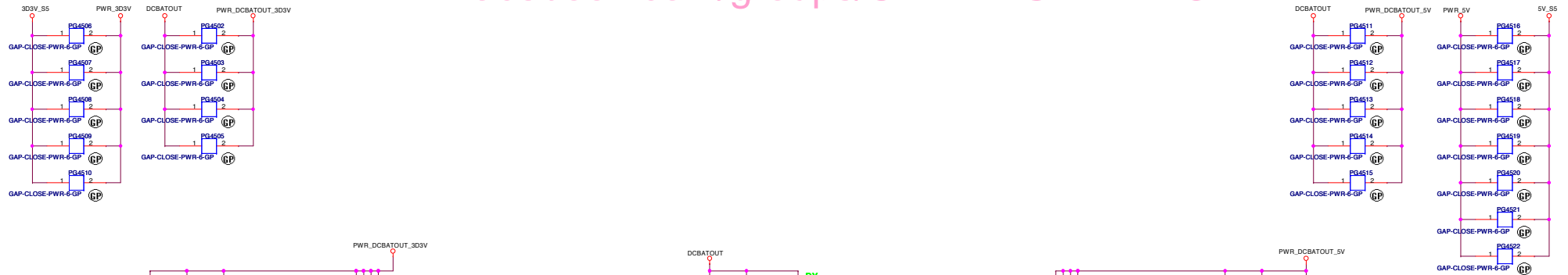
SSID = Charger

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	Site	PR13L3F_A4	Adapter Current	AC_Present_percent (5%~120%)	AC_Present Current	Sense resistor	Current to PR4407	PR4401
4071	AC - Battery	W846	7.1	100%	2.12A	0.01000m	0.0000	4.0
4249	AC - Battery	W846	2.9	100%	2.92A	0.01000m	0.0000	4.0
4250	AC - Battery	W846	5.4	100%	5.40A	0.01000m	0.0000	4.0
5077	AC - Battery	W846	4.7%	100%	4.95A	10.0000m	0.0000	4.0
10077	AC - Battery	W846	6.3	100%	6.43A	10.0000m	0.0000	4.0
10377	AC - Battery	W846	7.1	100%	7.10A	10.0000m	0.0000	4.0

adapter 65W and 90W  
AC mode (default:120%):  
set up the value by PR4401 and PR4407

AC adapter detect current :  
Ac input current = 20 x (V<sub>acc</sub> - V<sub>acn</sub>) / 10mohm



Design Current : 5A  
OCP : 9A

Design Current : 7A  
OCP : 12A

$$V_{out} = 2 * (1 + R1/R2)$$

$$= 2 * (1 + 6.8K / 10K)$$

$$= 3.36V$$

$$V_{out} = 2 * (1 + R1/R2)$$

$$= 2 * (1 + 15.4K / 10K)$$

$$= 5.08V$$

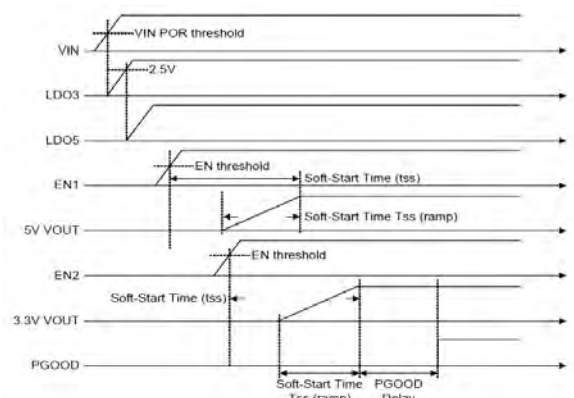
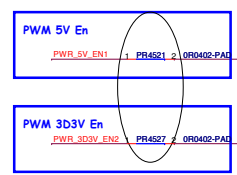


Figure 6. RT6575B Timing

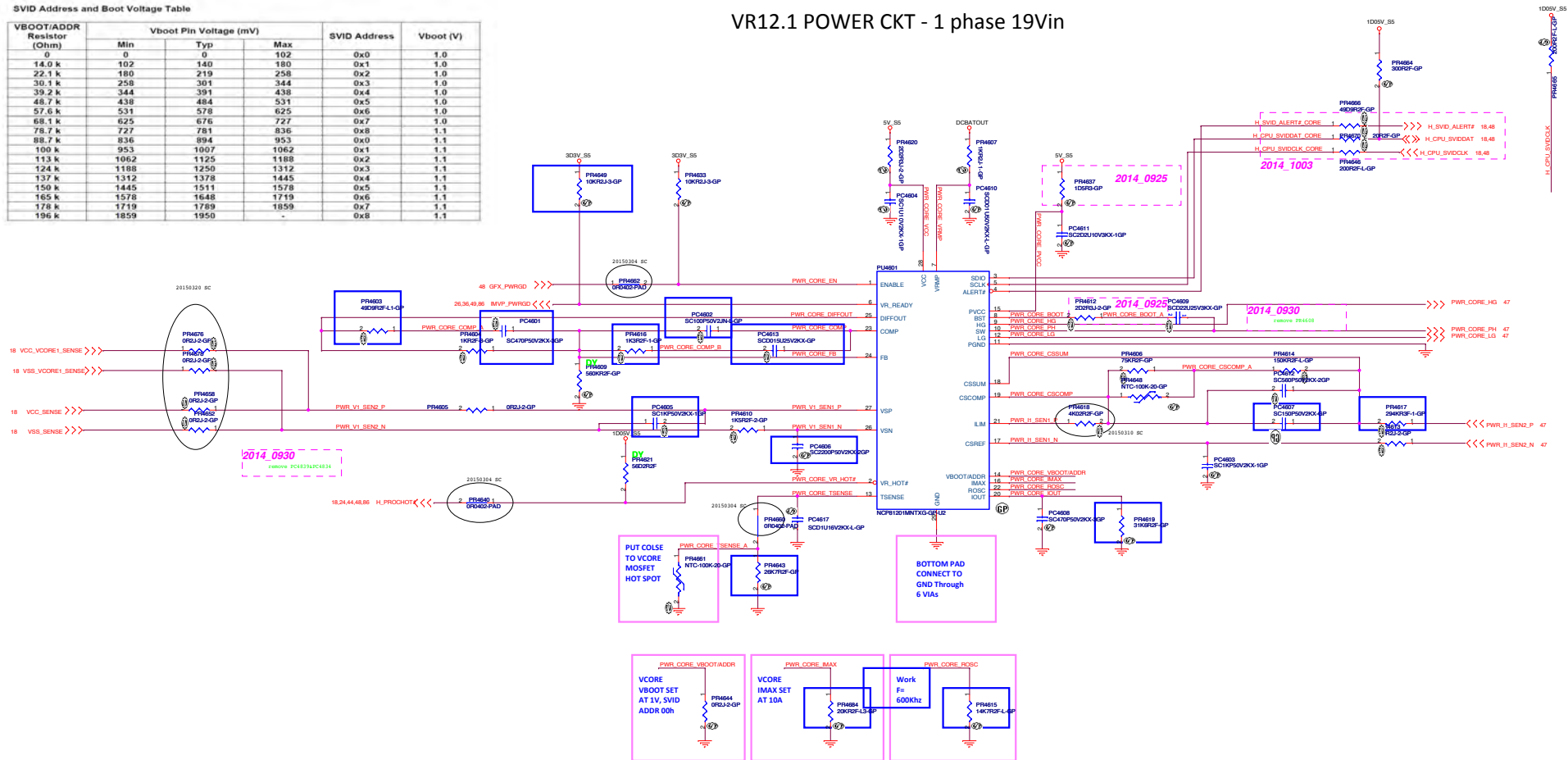


Vin POR threshold , Rising : 4.6 V ; Failing : 3.7 V  
EN threshold Logic-High : 1.6 V  
EN threshold Logic-Low : 0.4 V

## VR12.1 POWER CKT - 1 phase 19Vin

SVID Address and Boot Voltage Table

VBOOT/ADDR	Resistor	Min	Typ	Max	SVID Address	Vboot (V)
0		0	0	102	0x0	1.0
14.0 k		102	140	180	0x1	1.0
22.1 k		180	219	258	0x2	1.0
30.1 k		258	301	344	0x3	1.0
39.2 k		344	391	438	0x4	1.0
48.7 k		438	484	531	0x5	1.0
57.6 k		531	578	625	0x6	1.0
68.1 k		625	676	727	0x7	1.0
78.7 k		727	781	836	0x8	1.1
88.7 k		836	894	953	0x0	1.1
100 k		953	1007	1062	0x1	1.1
113 k		1062	1125	1188	0x2	1.1
124 k		1188	1250	1312	0x3	1.1
137 k		1312	1378	1445	0x4	1.1
150 k		1445	1511	1578	0x5	1.1
165 k		1578	1648	1719	0x6	1.1
178 k		1719	1789	1859	0x7	1.1
196 k		1859	1950	-	0x8	1.1



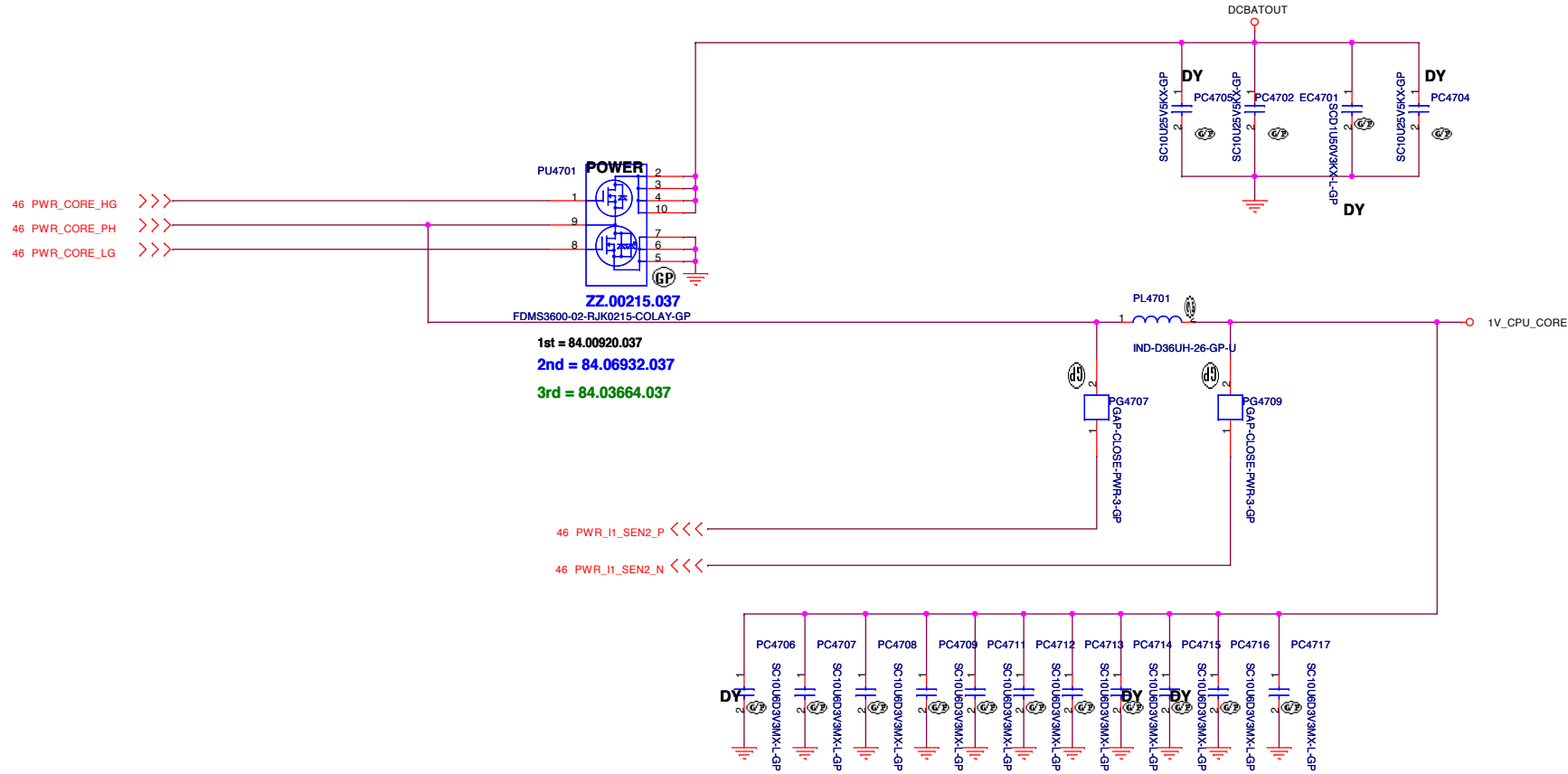
LA-T

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Taipei Hsien 301, Taiwan, R.O.C.

Rev: RT8171B CPUCORE(1/3)  
Doc: Domino  
Date: 1999/03/20, 2015 Sheet 46 of 102

SSID = CPU Regulator

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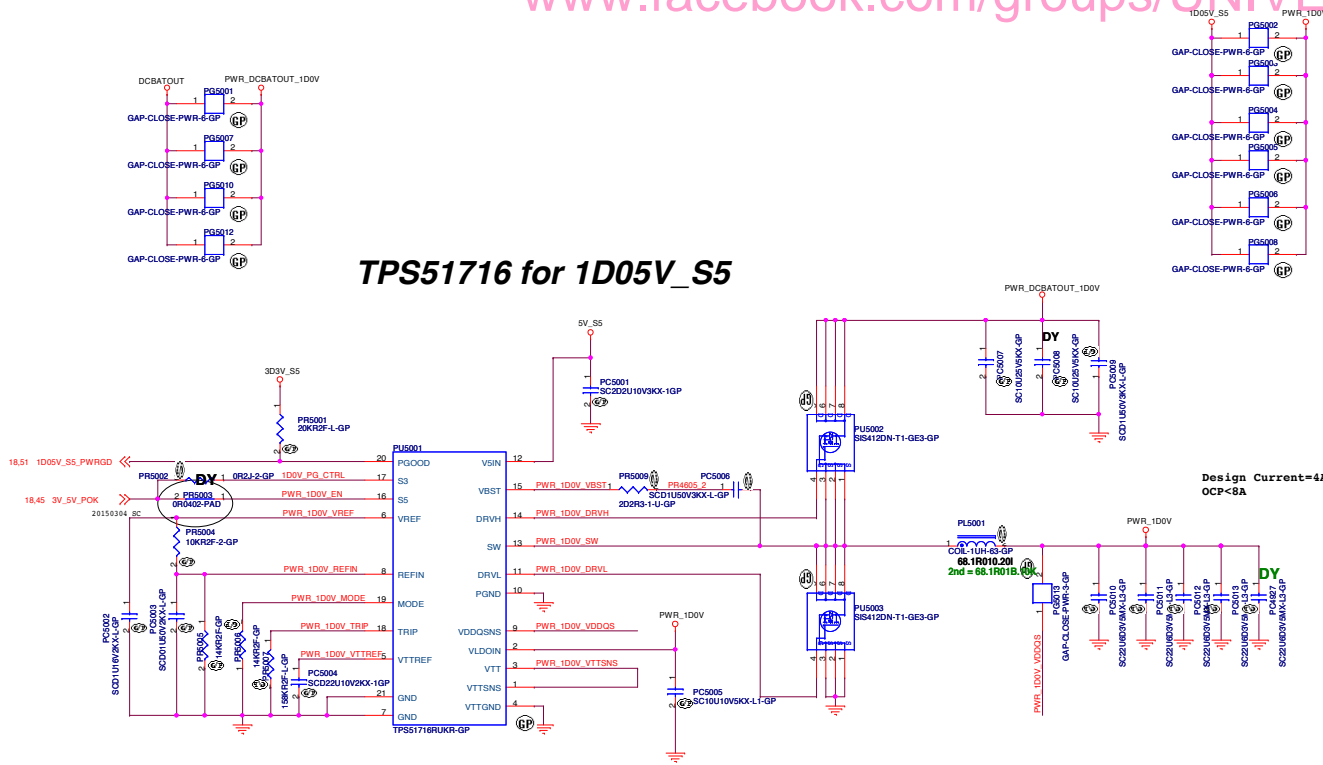
ULT



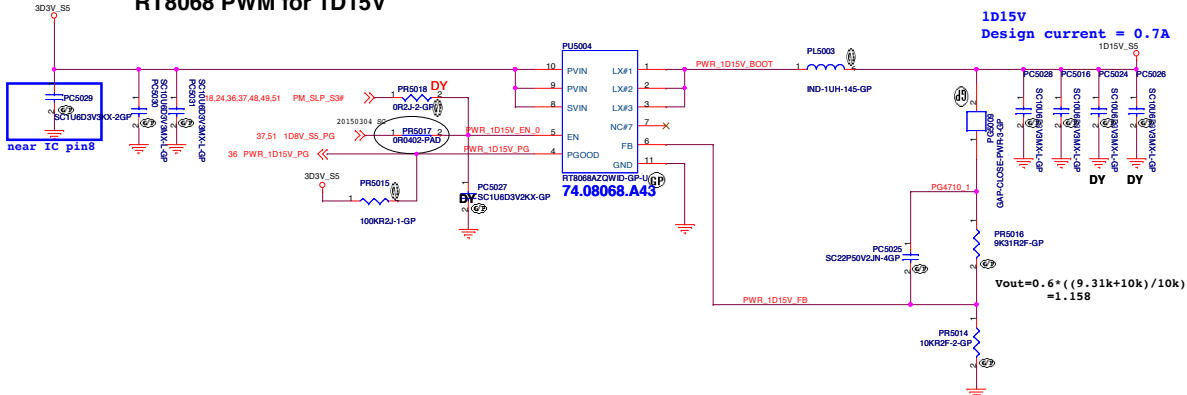




## TPS51716 for 1D05V\_S5

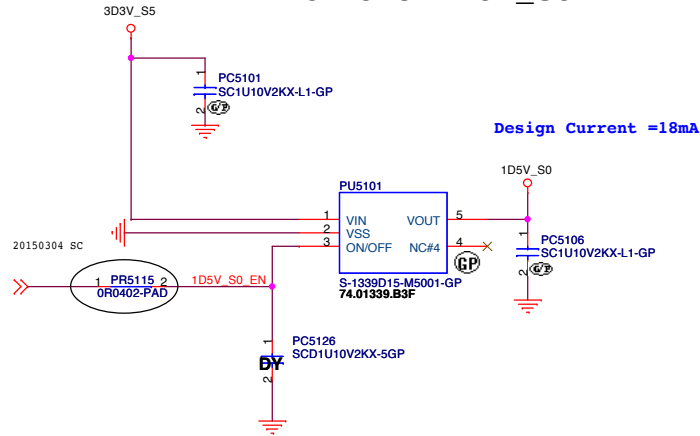


## RT8068 PWM for 1D15V

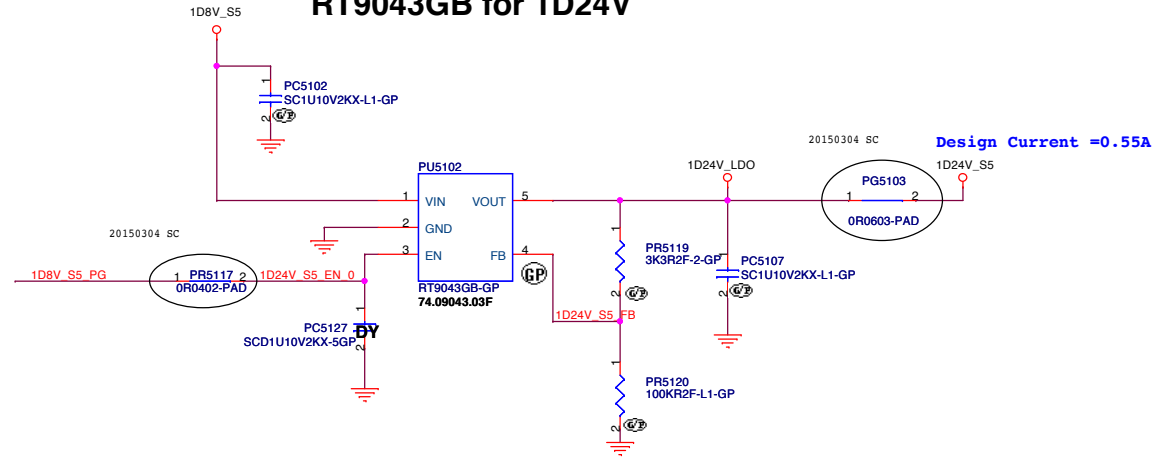


SSID = PWR.Plane.Regulator\_1p5v

### TLV70215 for 1D5V\_S0

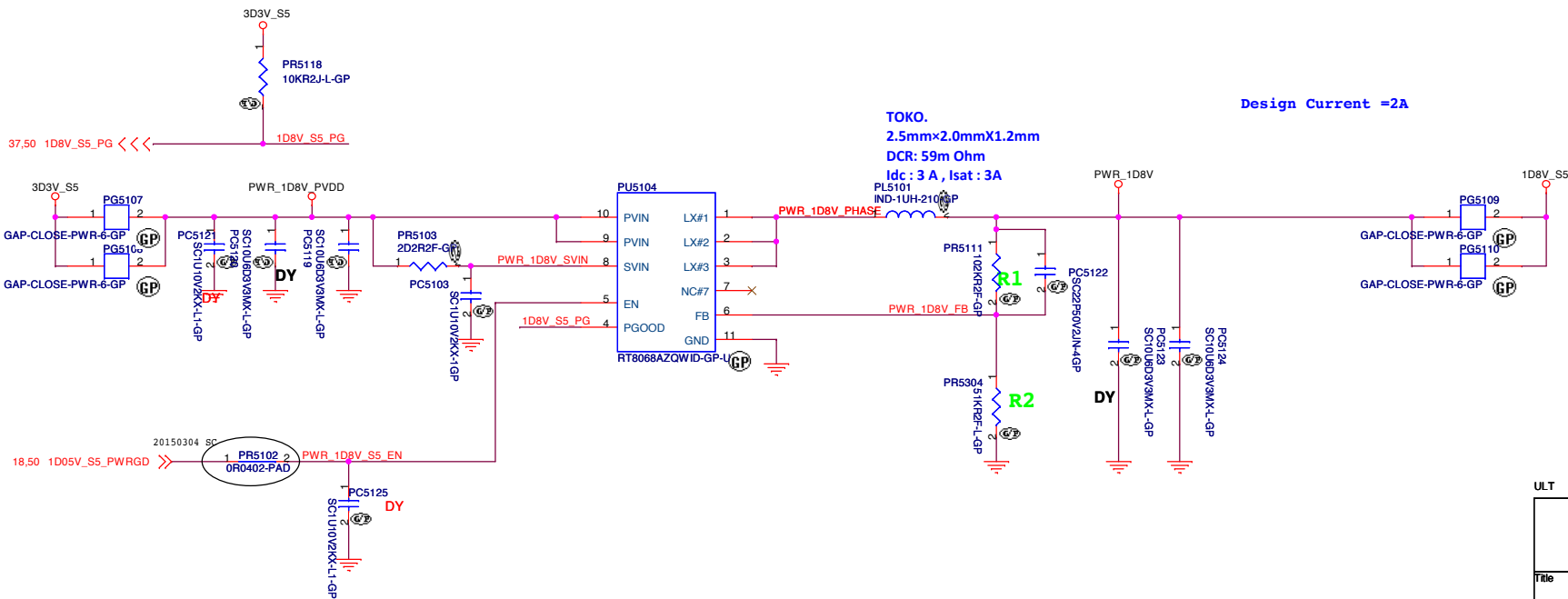


### RT9043GB for 1D24V



SSID = PWR.Plane.Regulator\_1p8v

### RT8068AZQWID-GP-U for 1D8V\_S5





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Title

CRT Connector

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-1

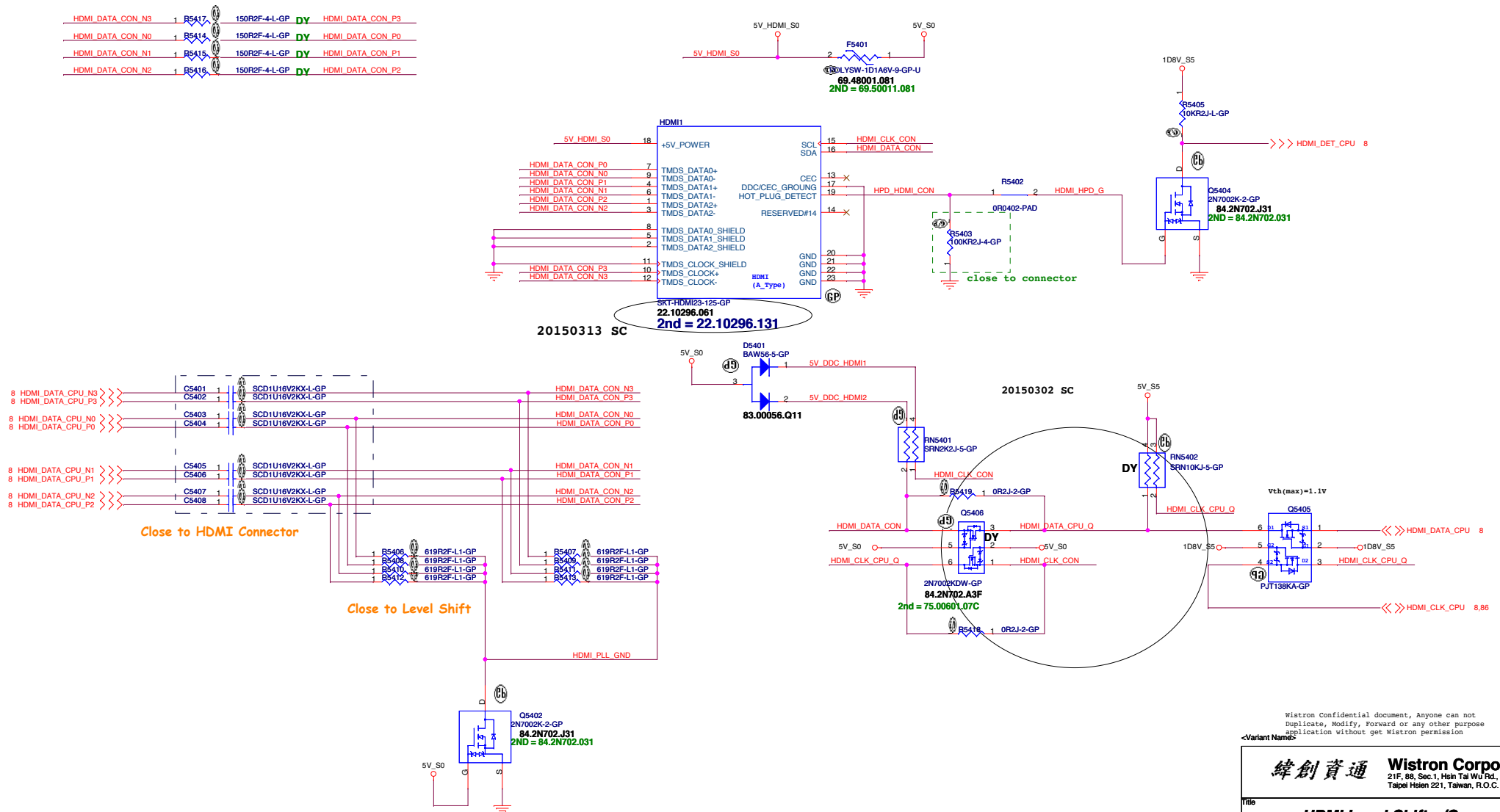
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Sheet 53 of 102

SSID = VIDEO

# HDMI Level Shifter & CONNECTOR

HDMI CONN



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Title		HDMI Level Shifter/Connector	
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Date	Friday, March 20, 2015	Sheet	54 of 102

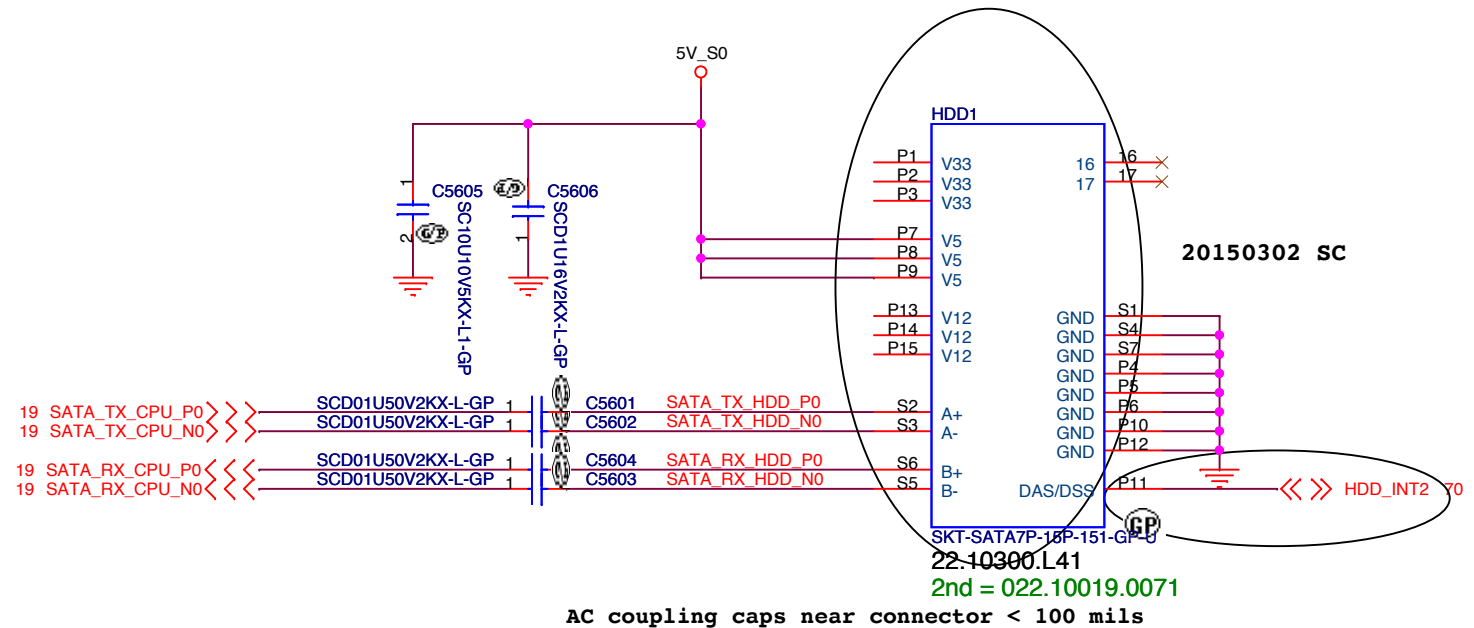
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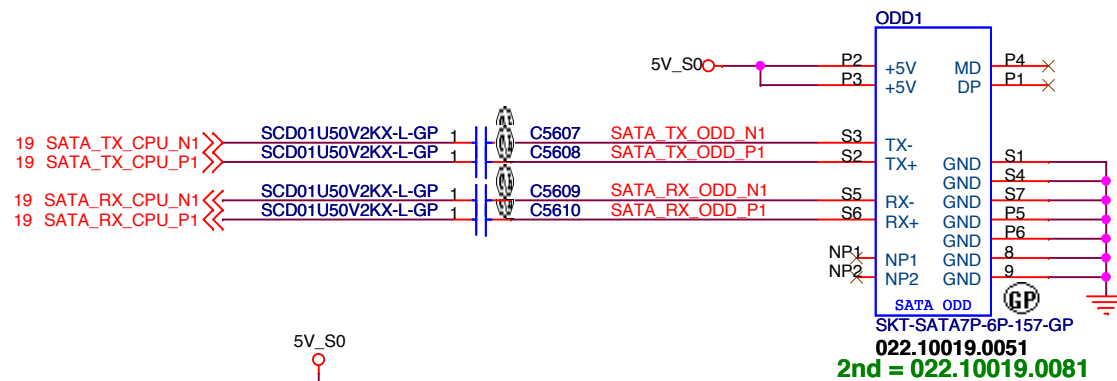
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hschih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reserved			
Size A3	Document Number		Rev -1
Date: Friday, March 20, 2015	Sheet 55 of 102		

SSID = SATA

# SATA HDD Connector



## ODD Connector

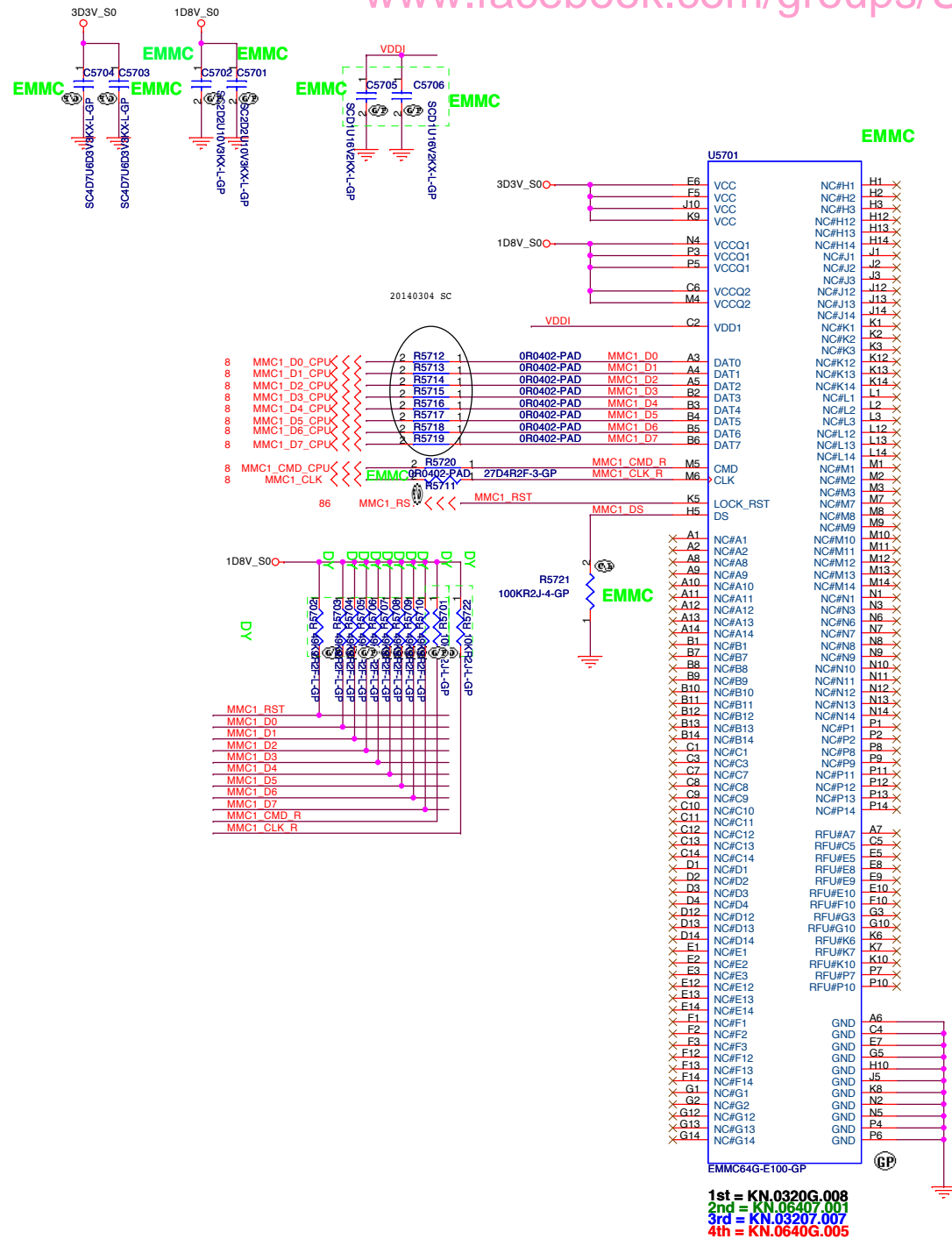


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<Variant Name>

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Title			
HDD / ODD / NGFF SSD			
Size A4	Document Number		Rev
	Domino		-1
Date:	Friday, March 20, 2015	Sheet 56	of 102

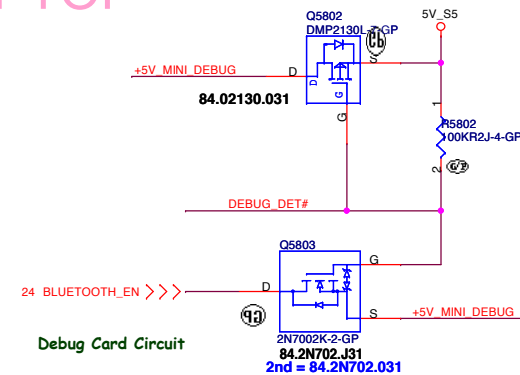




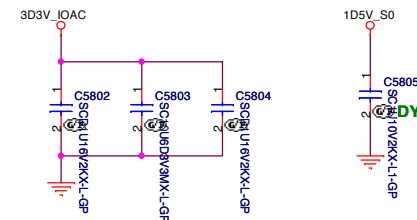
<Variant Name>

**SSID = Wireless** *Mini Card Connector(802.11a/b/g/n)*

**SSID = Wireless** *Mini Card Connector(802.11a/b/g/n)*



## Debug Card Circuit



**<Variant Name>** applicat

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### **MINICARD(WLAN)**

Rev

1

Sheet 58 of 102

SSID = 3G

# Mini Card Connector(WWAN)

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Title

**WWAN CONN**

Size  
A4

Document Number

**Domino**

Rev  
**-1**

Date: Friday, March 20, 2015

Sheet 59 of 102

SSID = mSATA

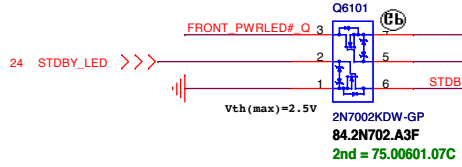
www.facebook.com/groups/UNIVERSELAPTOP  
*Mini Card Connector(mSATA)*

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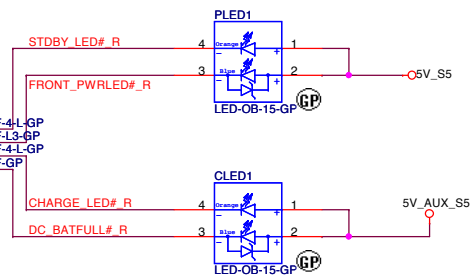
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Domino</div>	Rev <div>-1</div>
Date: Friday, March 20, 2015		Sheet 60 of 102

Power button LED

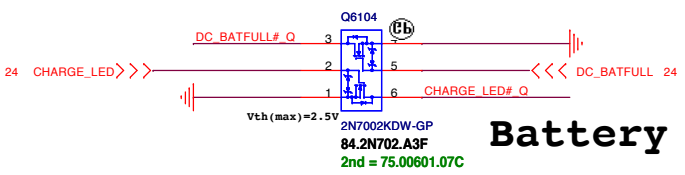


Power STDBY\_LED

- STDBY\_LED#\_Q 1 R6101 150R2F-4-L-GP
- FRONT\_PWRLED#\_Q 1 R6102 100R2F-L3-GP
- CHARGE\_LED#\_Q 1 R6103 150R2F-4-L-GP
- DC\_BATFULL#\_Q 1 R6104 249R2F-GP



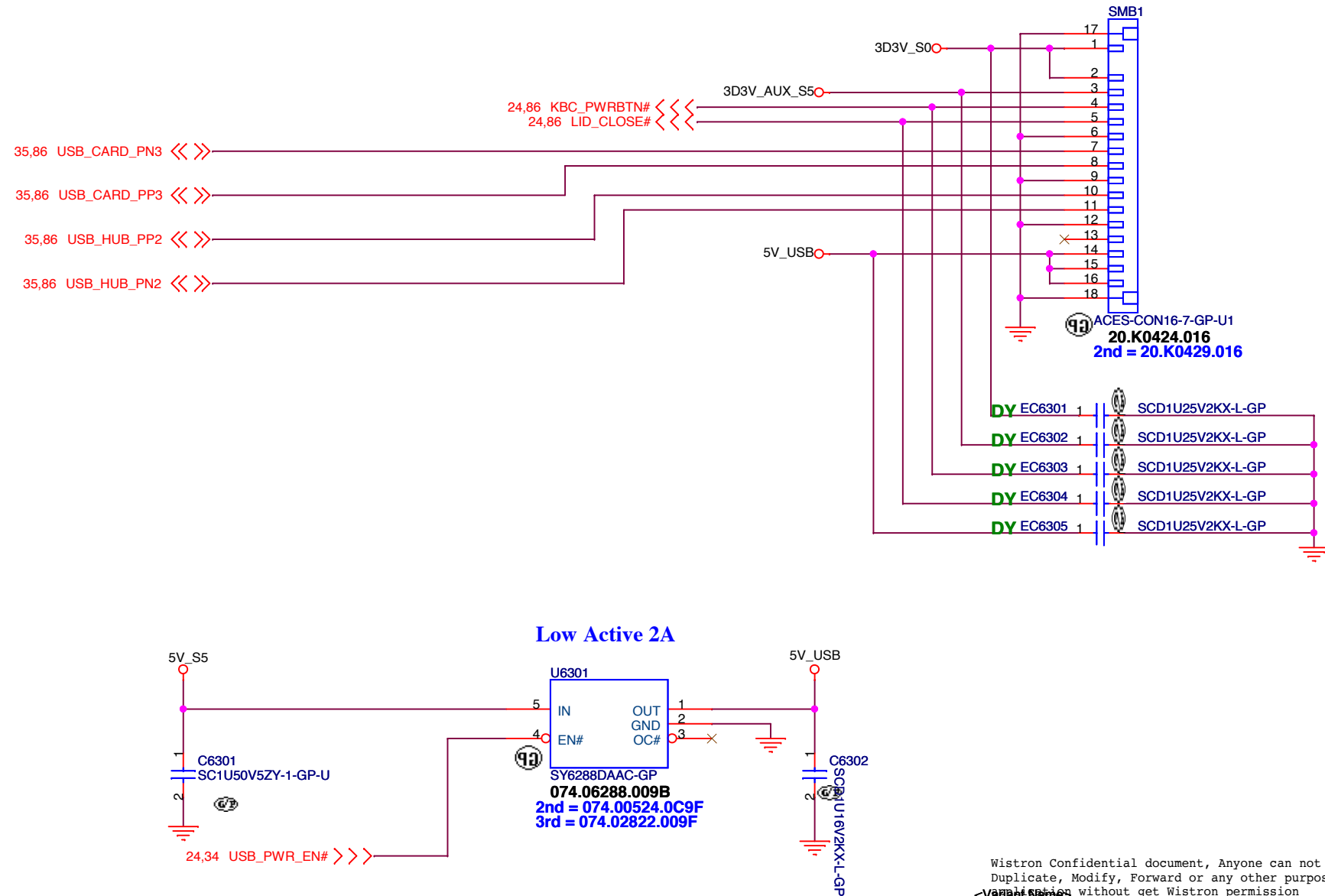
Battery LED2(DC\_BATFULL)



Battery LED1(CHARGE)

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Title			
<b>Key Board/Touch Pad</b>			
Size B	Document Number		Rev
	<b>Domino</b>		<b>-1</b>
Date:	Friday, March 20, 2015	Sheet 62	of 102



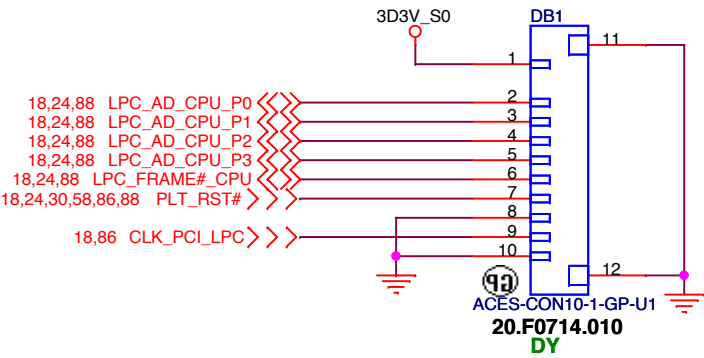
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<b>Title</b> <b>IO Board Connector</b>			
<b>Size</b> A4	<b>Document Number</b> <b>Domino</b>		<b>Rev</b> <b>-1</b>
<b>Date:</b> Friday, March 20, 2015		<b>Sheet</b> 63	<b>of</b> 102

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Title <div>Hall Sensor</div>		
Size <div>A4</div>	Document Number <div>Domino</div>	Rev <div>-1</div>
Date: Friday, March 20, 2015		Sheet 64 of 102





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Title		
Dubug connector		
Size	Document Number	Rev
A4	Domino	-1
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Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>Domino</div>	Rev <div>-1</div>
Date: Friday, March 20, 2015		Sheet 66 of 102

## Free Fall Sensor

### Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

# Blanking

**SDO="H"; address="3Ah"**  
**\*SDO="L"; address="38h"**

**\*CS="H"; mode="I2C"**  
**CS="L"; mode="SPI"**

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Title

**G Sensor**

Size  
A

Document Number

**Domino**

Rev

**-1**

Date: Friday, March 20, 2015

Sheet 67 of 102

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Title		
Thunderbolt (1/5)		
Size	Document Number	Rev
A4	Domino	-1
Date: Friday, March 20, 2015		Sheet 68 of 102

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Title <b>Thunderbolt (2/5)</b>		
Size A4	Document Number <b>Domino</b>	Rev <b>-1</b>
Date: Friday, March 20, 2015		Sheet 69 of 102

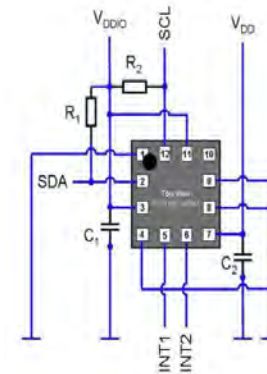
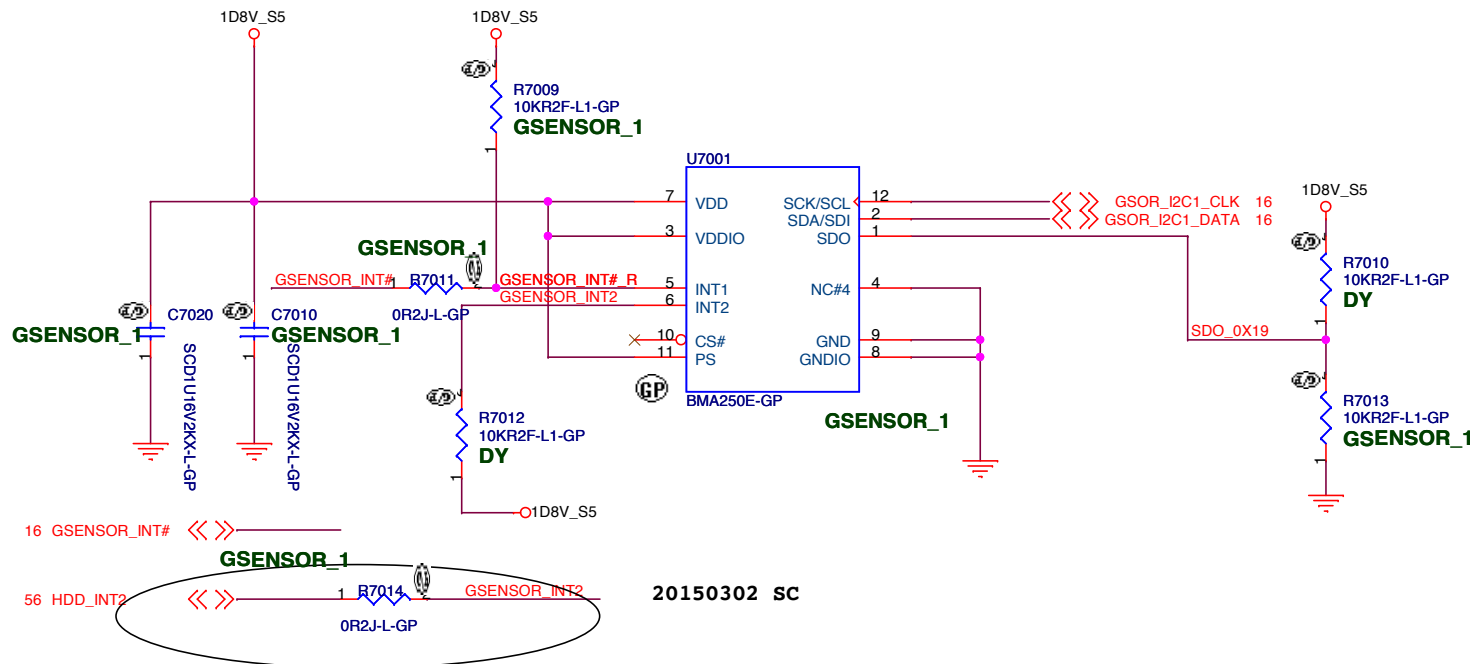
**SSID = User.Interface**

## G Sensor

### Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

The default I<sup>2</sup>C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V<sub>DDIO</sub>'.



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Title

**GSENSOR**

Size Custom

Document Number

**Domino**

Rev

**-1**

Date: Friday, March 20, 2015

Sheet 70

of

102

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Title

Thunderbolt (4/5)

Size

A4

Document Number

Domino

Rev

-1

Date: Friday, March 20, 2015

Sheet 71 of 102

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Title			
<b>Thunderbolt (5/5)</b>			
Size A4	Document Number <b>Domino</b>		Rev <b>-1</b>
Date: Friday, March 20, 2015		Sheet 72 of	102





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Title			
GPU (DIGITALOUT)			
Size	Document Number	Rev	
Custom	Domino	-1	
Date:	Friday, March 20, 2015	Sheet	74 of 102



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GPU (GPIQ/STRAP)			
Doc	Document Name	Rev	-1
Doc	Doc	Doc	Doc
Domino			
Doc		Doc	Doc



<Variant Name>

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Title

**GPU-VRAM1,2 (1/4)**

Size  
Custom

Document Number

Rev

**Domino****-1**

Date

Friday, March 20, 2015

Sheet

78

of

102

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Title		
GPU-VRAM3,4 (2/4)		
Size	Document Number	Rev
A3	Domino	-1
Date:	Friday, March 20, 2015	Sheet 79 of 102

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Title			
GPU-VRAM5,6 (3/4)			
Size	Document Number		Rev
A3	Domino		-1
Date:	Friday, March 20, 2015	Sheet	80 of 102



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Title			
<b>GPU-VRAM7,8 (4/4)</b>			
Size	Document Number		Rev
A3	<b>Domino</b>		<b>-1</b>
Date:	Friday, March 20, 2015		Sheet 81 of 102

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Title

RT8812A VGA CORE

Size

Document Number

Rev

Date: Friday, March 20, 2015

Domino

-1

Sheet 82 of 102

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Title		DISCRETE VGA POWER	
Size	Document Number	Rev	
Custom	Domino	-1	
Date	Friday, March 20, 2015	Sheet	83 of 102

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Title		
Switchable GFX LCD(1/2)		
Size	Document Number	Rev
A4	Domino	-1
Date: Friday, March 20, 2015		Sheet 84 of 102

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>Switchable GFX LCD(2/2)</b>		
Size A4	Document Number <b>Domino</b>	Rev <b>-1</b>
Date: Friday, March 20, 2015	Sheet 85 of	102



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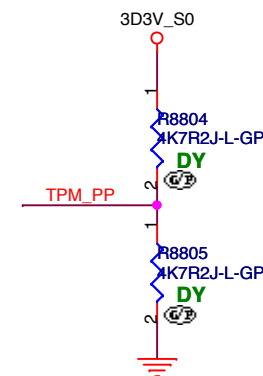
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Title **Reserved**

Size A4	Document Number <b>Domino</b>	Rev <b>-1</b>
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Sheet 88 of 102



SSID = Finger Print

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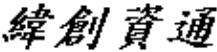
Title **Reserved**

Size A4	Document Number <b>Domino</b>	Rev <b>-1</b>
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SSID = Express Card

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Title <b>Reserved</b>			
Size A4	Document Number <b>Domino</b>		Rev <b>-1</b>
Date: Friday, March 20, 2015		Sheet 90 of	102

SSID = Smart Card

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Title

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Size  
A4

Document Number

**Domino**

Rev  
**-1**


Date: Friday, March 20, 2015

Sheet 91 of 102

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Title <b>Reserved</b>			
Size A4	Document Number <b>Domino</b>		Rev <b>-1</b>
Date: Friday, March 20, 2015		Sheet 92 of	102

SSID = Docking

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Title			<b>Reserved</b>	
Size A4	Document Number <b>Domino</b>			Rev <b>-1</b>
Date: Friday, March 20, 2015		Sheet	93	of 102

SSID = Intel LAN

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Title		
Reserved		
Size A4	Document Number Domino	Rev -1
Date: Friday, March 20, 2015		Sheet 94 of 102

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Title			
<b>LAN Switch</b>			
Size A4	Document Number		Rev <b>-1</b>
Date: Friday, March 20, 2015		Sheet 95 of	102

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 <sup>1</sup>	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# <sup>1</sup>	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 <sup>1</sup>	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# <sup>1</sup>	O	System	18	HOOK7	DBR# <sup>1</sup>	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Title

PCH XDP

Size A4

Document Number

Rev -1

Date: Friday, March 20, 2015


Sheet 96 of 102

Domino



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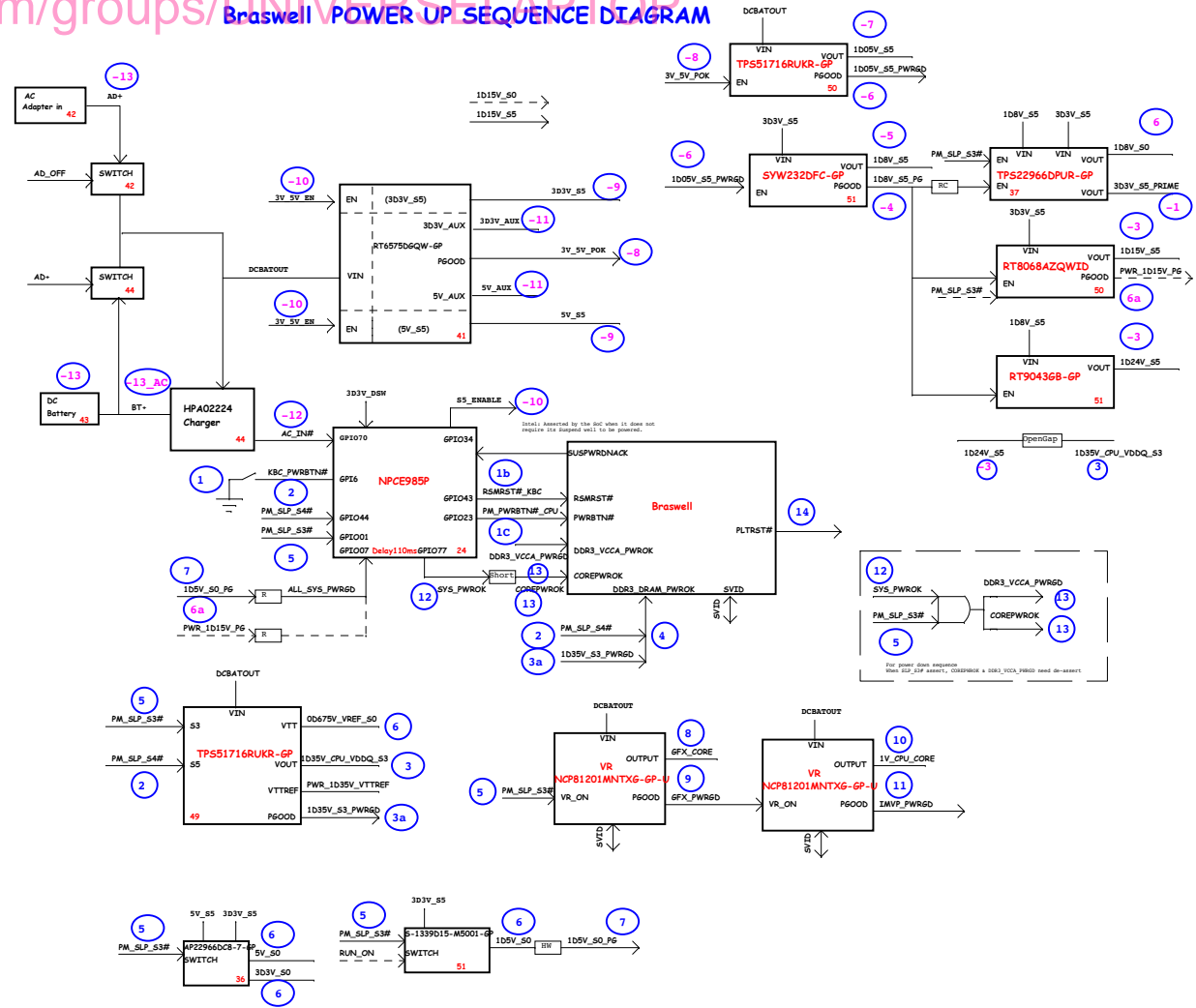
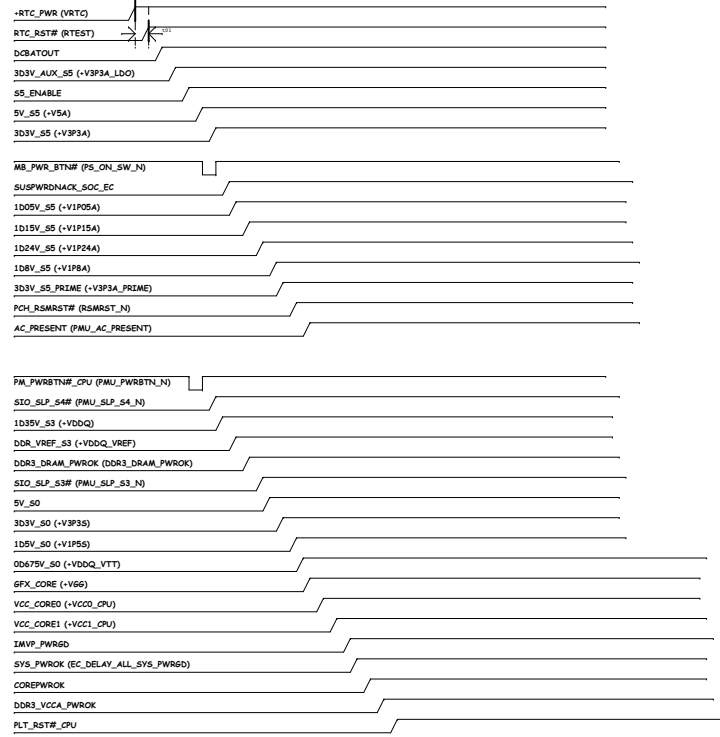
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>table of content</i></b>			
Size A4	Document Number <b>Domino</b>		Rev <b>-1</b>
Date:	Friday, March 20, 2015	Sheet 97 of	102

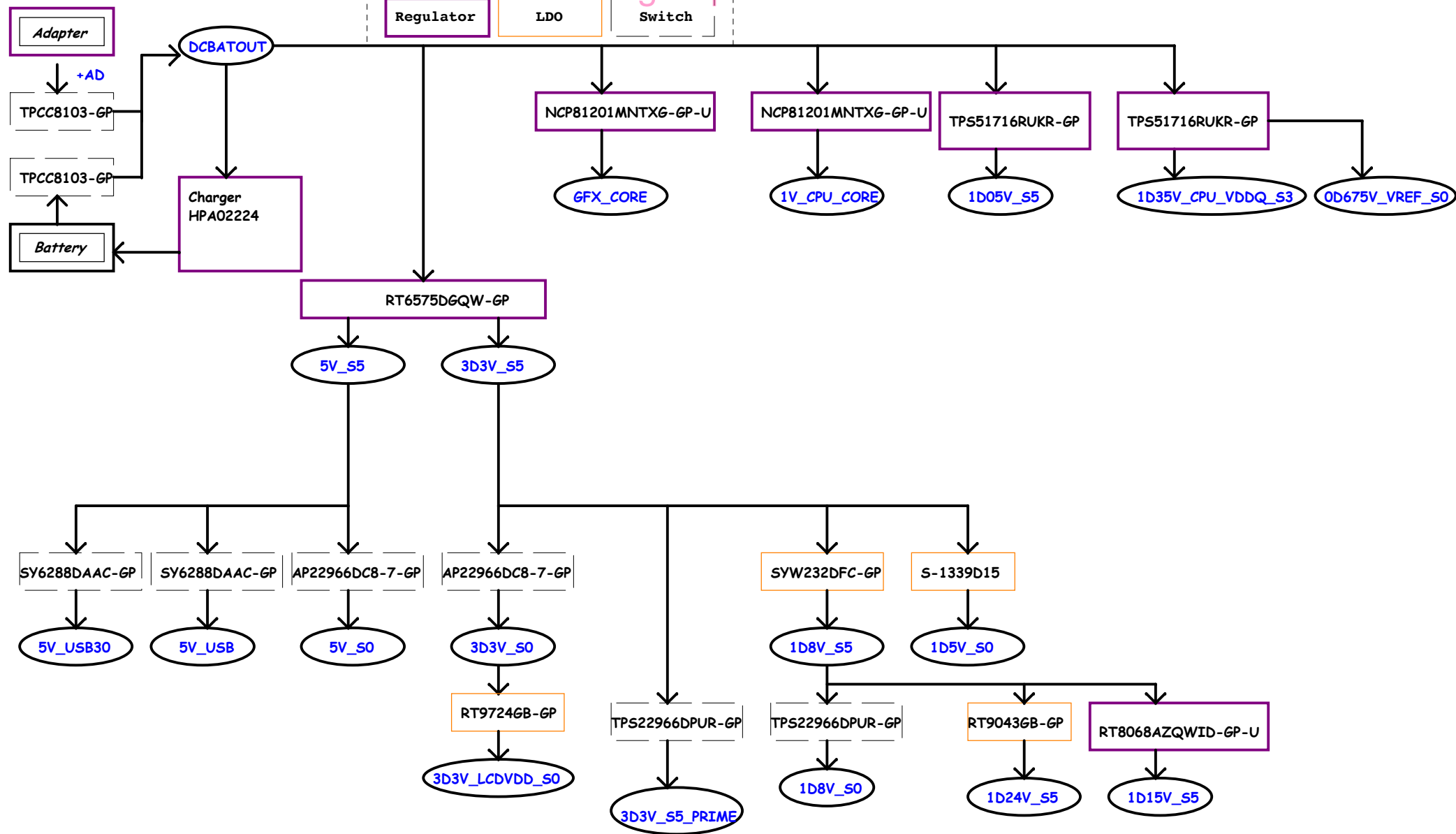
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Title		
Change History		
Size A4	Document Number Domino	Rev -1
Date: Friday, March 20, 2015		Sheet 98 of 102

# Intel-Power Up Sequence

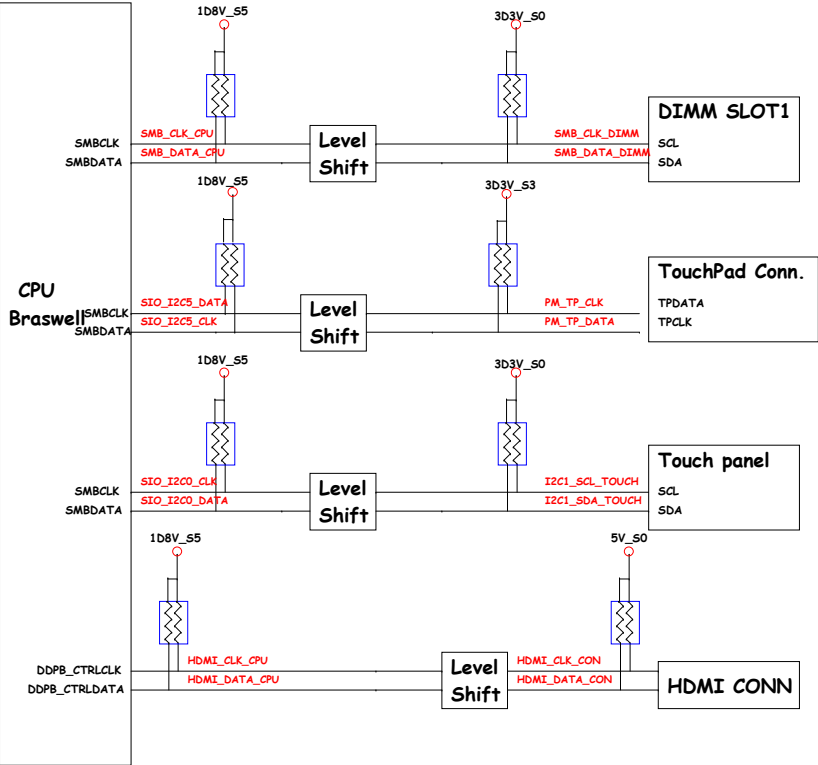
## (AC mode)



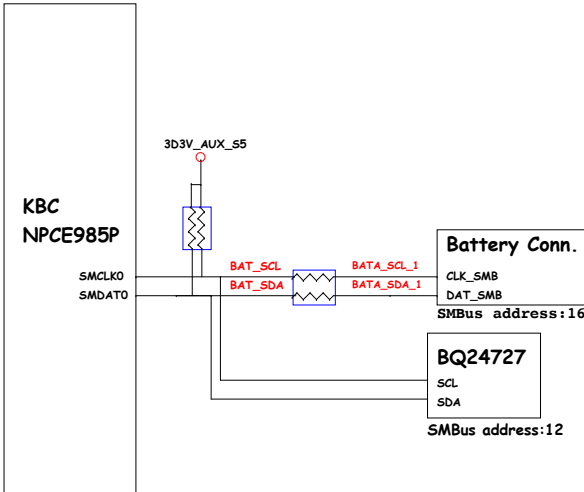


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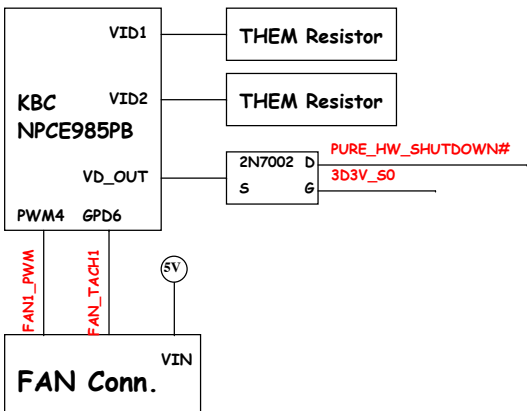
PCH SMBus Block Diagram



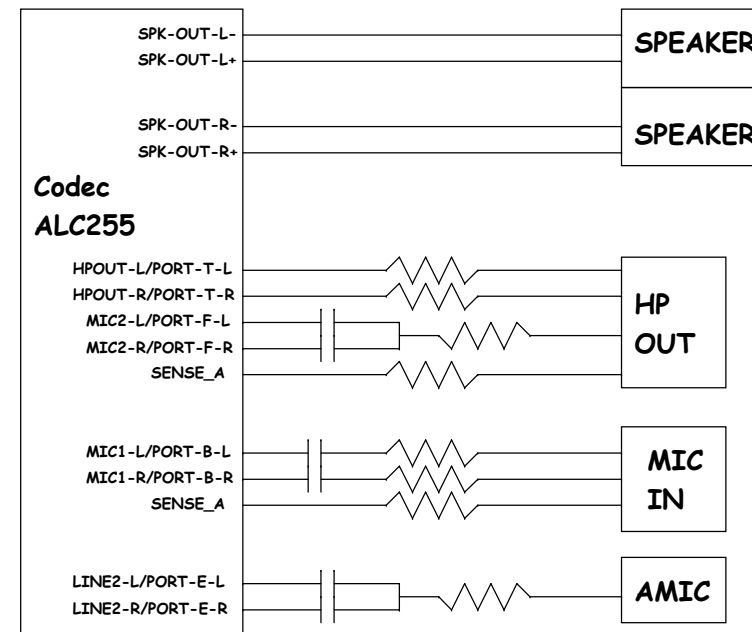
KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



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<Variant Name>

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Title <b>THERMAL/AUDIO BLOCK DIAGRAM</b>			
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Date: Friday, March 20, 2015	Sheet 102 of 102		